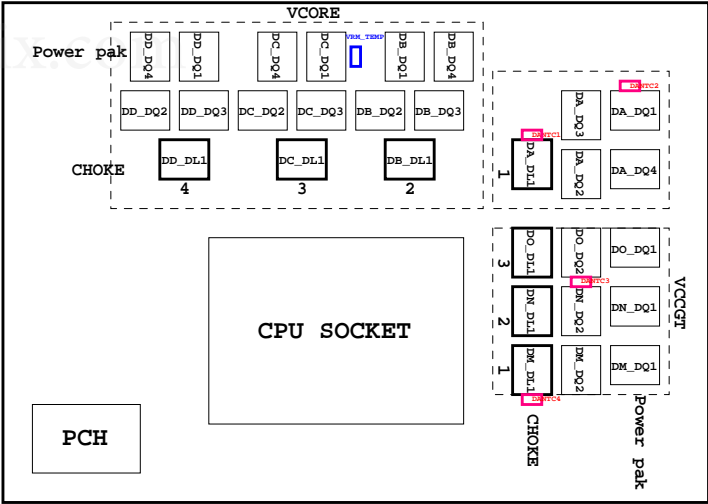


01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1151-A (CFL_R0.4)
05	CPU_LGA1151-B-DDR4 (CFL_R0.4)
06	CPU_LGA1151-C-Z系列 (CFL_R0.4)
07	CPU_LGA1151-D (CFL_R0.4)
08	DDR 4 CHANNEL A (CFL_R0.1)
09	DDR 4 CHANNEL B (CFL_R0.1)
10	PCH CLOCK BUFFER (REV0.6)
11	PCH DMI,USB,PCIE
12	PCH MISC
13	PCH SATA,PCIE,SATA_EXPRESS
14	PCH PWR
15	PCH GND
16	Dual BIOS (CFL_R0.4)
17	I/O ITE8628 (CFL_R0.4)
18	HWM (CFL_R0.4)
19	FAN CTRL-CFL-SIO_4 FAN (CFL_R0.2)
20	PCIEX16 SLOT (REV0.2)
21	PCIEX4 SLOT1 (REV0.51)
22	PCIEX4 SLOT2 (REV0.51)
23	PCIEX1*2 SLOT (REV0.51)
24	M.2 x4 (REV0.6)
25	SATA
26	VCORE_ ISL95866(PWM) (CFL_R0.32)
27	VCORE_ ISL95866(Vcore) (CFL_R0.32)
28	VCORE_ ISL95866(VccGT) (CFL_R0.32)
29	VCCSA_VCCIO-合金-Z系列 (CFL_R0.41)
30	RT8120_DDR_CHOKE-IRON-2L (CFL_R0.4)
31	RT8120_VPP_CHOKE-合金 (CFL_R0.4)
32	RT8120_PCH (CFL_R0.4)
33	DISCRETE POWER (REV0.51)
34	CPU POWER-Z系列 (CFL_R0.42)
35	NCP3933 OVER VOLTAGE
36	ATX POWER , -PROCHOT

37	KB_MS_USB (CFL_R0.2)
38	DVI (CFL_R0.2)
39	R_USB30 (CFL_R0.2)
40	INETL I219V (CFL_R2.01)
41	USB30_LAN CONNECTOR-I219V (CFL_R2.01)
42	ALC892-GR CODEC (CFL_R2.04)
43	REAR AUDIO JACK (CFL_R2.04)
44	F_USB30 (CFL_R0.2)
45	F_USB20 (CFL_R0.2)
46	COM , LPT , TPM (CFL_R0.2)
47	F_PANEL (CFL_R0.2)
48	HDMI (CFL_R0.2)
49	IDT6V41630_CLK BUFFER (REV0.1)
50	Audio / DEBUG / XMP LED (CFL_R2.01)
51	EMI-ESD (CFL_R0.1)
52	POWER MAP
53	TABLE LIST



*rev 1.0*

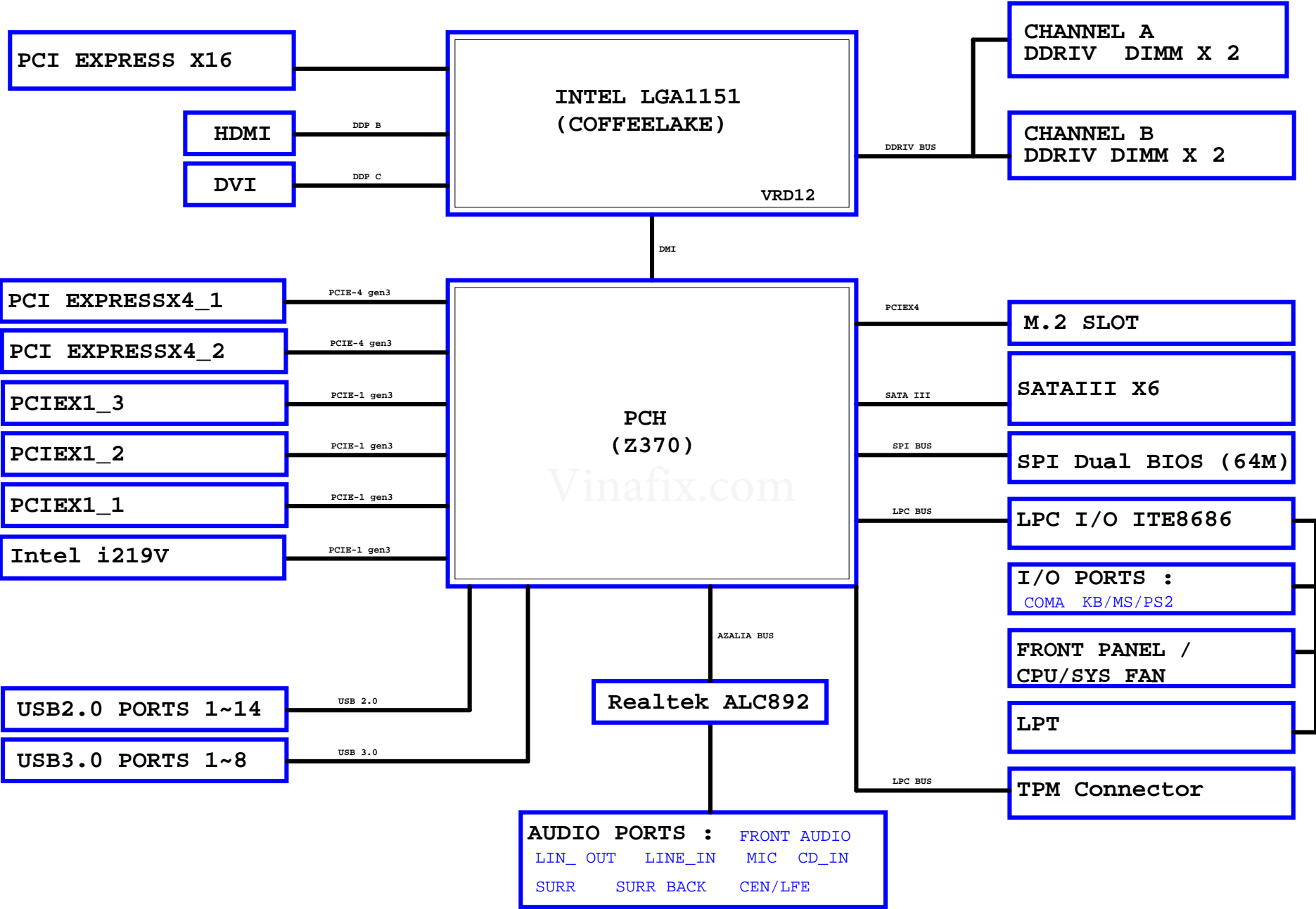
## Component value change history

Data	Change Item	Reason
2017/06/08	first release	
	9MZ370HD3-00-01 BOM	
2017/07/28	9MZ370HD3-00-02 BOM	
	1.Add OR20,OR21,OR19,OQ15,OQ14 , OR205->00hm	
	2.OR33->X , OR35上件 3.BSR1,BSR5->330/4 4.DA_DC7,DA_DC8,DB_DC7, DB_DC8,DC_DC7,DC_DC8,DD_DC7,DD_DC8->33p 5.PCIEX16->11AC1-023164-G1R	
	6.PCIEX4_1,PCIEX4_2->11AC1-023065-51R 7. BSR1,BSR5->330/4	
	8.DA_DC7,DA_DC8,DB_DC7,DB_DC8,DC_DC7,DC_DC8,DD_DC7,DD_DC8,DM_DC1,DN_DC1,DO_DC1->X	
	9.PCIEX16->11AC1-023164-G1R,PCIEX4_1,PCIEX4_2->PCI-E/4X-66P/GY/LONG DOUBLE/HK*2	
	10.DAR37->2K,DAR35->6.2K,DAC14->100P,DAC23->1.5n,DAR63->3.65K, ,DAR52->100K,DAR44->576,DAC12->X,DAC43->0.22u,DAR72->46.4K, ,DAC34->X,DAR41->6.98K,DAR71->267,DAC44->0.22u 11.DA_DL1,DB_DL1,DC_DL1, ,DD_DL1,DM_DL1,DN_DL1,DO_DL1,DAL1-> 11LC5-M5300C-01R Footprint:CHOKE0U3-R30M-JJ3W	
	12.DAC22->8.2n 13.CR67,CR68,CR69,CR70,CR43,CR27->X 14.OR17,OR5,OQ10->X	
	15.M_BIOS->10HP4-112564-50R, B_BIOS->10HP4-112564-51R	
	16.DAC43->0.1u,DAC34->0.047u,DAC44->0.1u,DAC23->1.2n	
	17.DAR47->15.4K , DAR67->13.3K ,18.PCH->10HB1-03Z370-20R	
	19.PCH_HS->12SP2-S08607-01R/02R/03R,TMOS->12SP2-S09426-11R/12R/13R, RMOS->12SP2-S08026-11R/12R/13R 20.PCIEX16->PCI-E/16X-164P/GY/LONG DOUBLE/HK*2	
	21.DDR4_4,DDR4_3->DDR4/288/BK/VA/D/GF/TWO LATCH/C7025	
	DDR4_1,DDR4_2->DDR4/288/GY/VA/D/GF/TWO LATCH/C7025	
2017/08/14	9MZ370HD3-00-10A BOM	
	1.M_BIOS , B_BIOS->64M/Q/SPI/S08/S,BSR21,BSR22->X 2.OR1,OR18,OR4,OR16 ,OR2,OQ9,OQ13,OR6,OR13,OQ11,OQ12->X,WR8->X 3.10SL2-000008-31R/X	
	4.Q9->EMF30N02J/SOT23/627pF/30m 5.CEC7,CEC9,CEC10,CEC11->X	
	6.DAR47->14.3K,TMOS->12SP2-S09426-21R/22R/23R,RMOS->12SP2-S08026-21R/22R/23R	
2017/08/15	9MZ370HD3-00-10B BOM	
	1. M_BIOS,B_BIOIS-> 128M/Q/SPI/S08/S	
2017/08/17	9MZ370HD3-00-10C BOM	
	1. DAR47->13.3K	

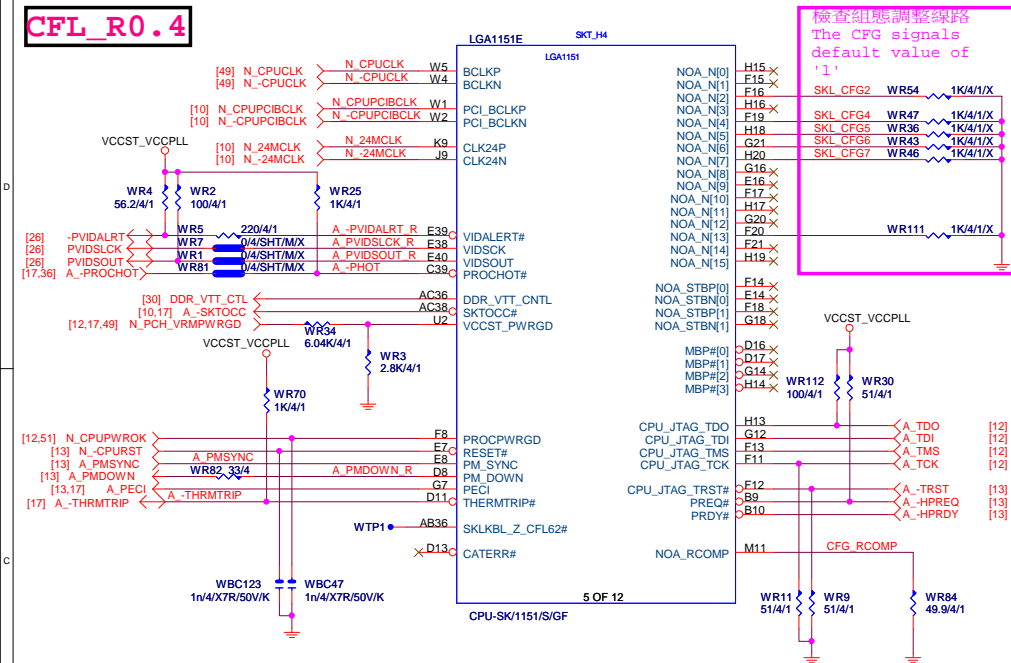
## Circuit or PCB layout change

[illegible]

BLOCK DIAGRAM



## CFL\_R0.4

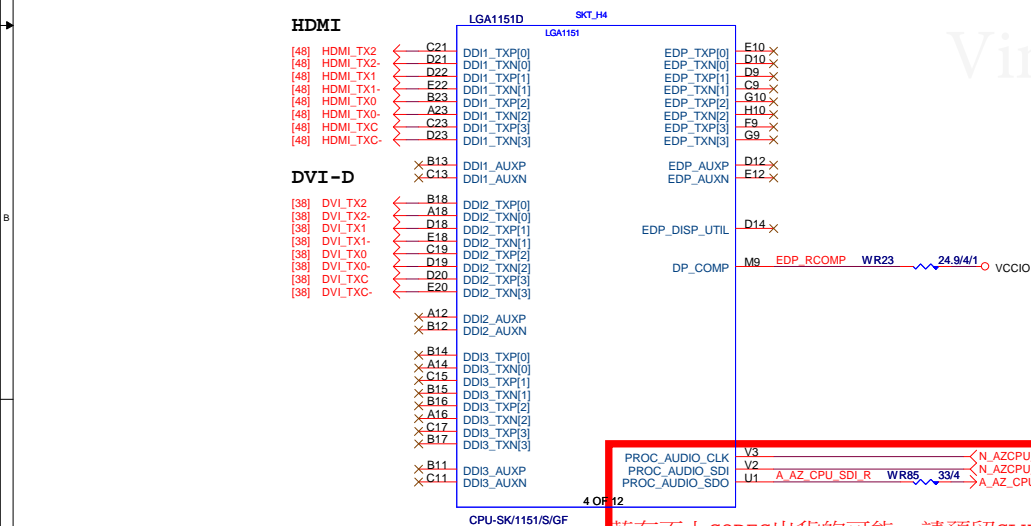
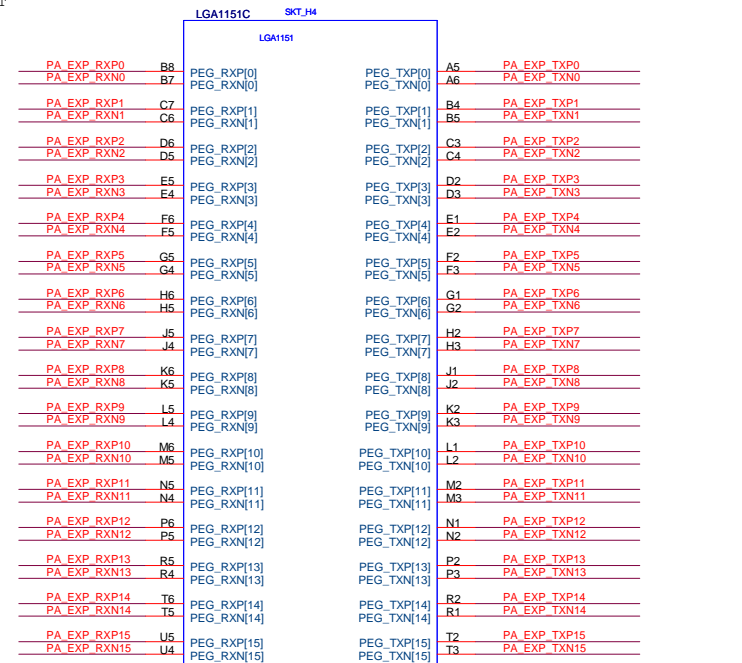


```
CFG[4]: 1=eDP enable / 0=eDP disable
CFG[7]: 1=PEG Train immediately following RESET
        0=PEG Wait for BIOS

CFG[13]: 1=VCCSA Fixed Mode / 0=SVID Mode
```

SKL\_CFG5 ,WR37  
非x8/x4/x4設計的可移除

Bifurcation Config.	Signals Lanes		
	CFG[6]	CFG[5]	CFG[2]
1x16	1	1	1
1x16 Reversed	1	1	0
2x8	1	0	1
2x8 Reversed	1	0	0
1x8+2x4	0	0	1
1x8+2x4 Reversed	0	0	0



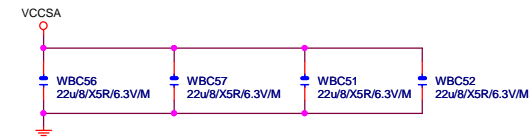
若有不上CODEC出貨的可能，請預留CLK and SDO對地電阻。

G-15u : (CPU-SK/1151/S/15)  
10SC1-F01151-11R / 10SC1-F01151-12R  
G-FL : (CPU-SK/1151/S/GF)  
10SC1-F01151-21R / 10SC1-F01151-22R

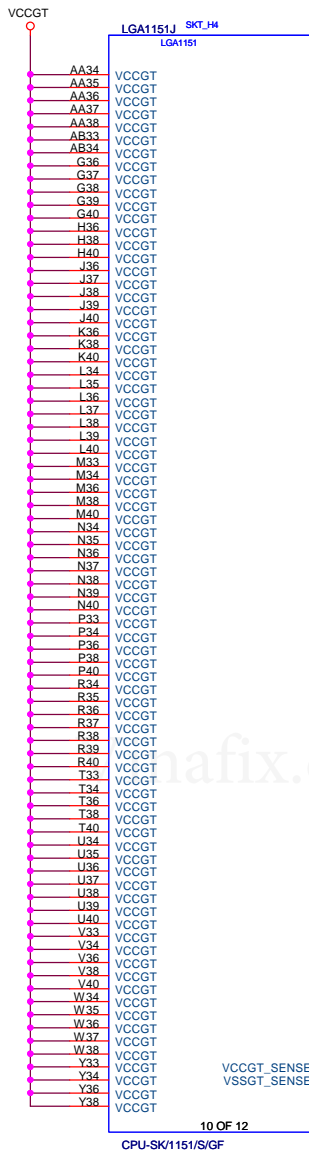
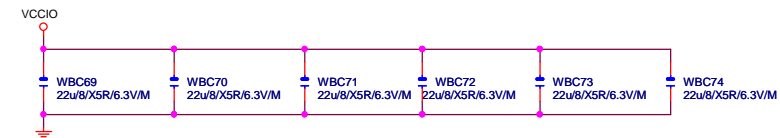
PA\_EXP\_TXP[0..15] >> PA\_EXP\_TXP[0..15] [20]  
PA\_EXP\_TXN[0..15] >> PA\_EXP\_TXN[0..15] [20]  
PA\_EXP\_RXP[0..15] >> PA\_EXP\_RXP[0..15] [20]  
PA\_EXP\_RXN[0..15] >> PA\_EXP\_RXN[0..15] [20]

LGA1151A										LGA1151B									
SKT_H4										SKT_H4									
LGA1151										LGA1151									
MDA0	AE38	DDR0_DQ[0]	DDR0_CKP[0]	AW18	M_DCLKA0	↔	M_DCLKA0	[8]		MD80	AD34	DDR1_DQ[0]/DDR0_DQ[16]	DDR1_CKP[0]	AM20	M_DCLKB0	↔	M_DCLKB0	[9]	
MDA1	AE37	DDR0_DQ[1]	DDR0_CKN[0]	AV18	M_DCLKA0	↔	M_DCLKA0	[8]		MD81	AD35	DDR1_DQ[1]/DDR0_DQ[17]	DDR1_CKN[0]	AM21	M_DCLKB0	↔	M_DCLKB0	[9]	
MDA2	AG38	DDR0_DQ[2]	DDR0_CKP[1]	AW17	M_DCLKA1	↔	M_DCLKA1	[8]		MD82	AG35	DDR1_DQ[2]/DDR0_DQ[18]	DDR1_CKP[1]	AP22	M_DCLKB1	↔	M_DCLKB1	[9]	
MDA3	AG37	DDR0_DQ[3]	DDR0_CKN[1]	AY17	M_DCLKA1	↔	M_DCLKA1	[8]		MD83	AH35	DDR1_DQ[3]/DDR0_DQ[19]	DDR1_CKN[1]	AP21	M_DCLKB1	↔	M_DCLKB1	[9]	
MDA4	AE39	DDR0_DQ[4]	DDR0_CKP[2]	AW16	M_DCLKA2	↔	M_DCLKA2	[8]		MD84	AE35	DDR1_DQ[4]/DDR0_DQ[20]	DDR1_CKP[2]	AN20	M_DCLKB2	↔	M_DCLKB2	[9]	
MDA5	AE40	DDR0_DQ[5]	DDR0_CKN[2]	AV16	M_DCLKA2	↔	M_DCLKA2	[8]		MD85	AE34	DDR1_DQ[5]/DDR0_DQ[21]	DDR1_CKN[2]	AN21	M_DCLKB2	↔	M_DCLKB2	[9]	
MDA6	AG39	DDR0_DQ[6]	DDR0_CKP[3]	AT16	M_DCLKA3	↔	M_DCLKA3	[8]		MD86	AG34	DDR1_DQ[6]/DDR0_DQ[22]	DDR1_CKP[3]	AP19	M_DCLKB3	↔	M_DCLKB3	[9]	
MDA7	AG40	DDR0_DQ[7]	DDR0_CKN[3]	AU16	M_DCLKA3	↔	M_DCLKA3	[8]		MD87	AH34	DDR1_DQ[7]/DDR0_DQ[23]	DDR1_CKN[3]	AP20	M_DCLKB3	↔	M_DCLKB3	[9]	
MDA8	AJ38	DDR0_DQ[8]		AY24	CKEA0	↔	CKEA0	[8]		MD88	AK35	DDR1_DQ[8]/DDR0_DQ[24]		AY29	CKEB0	↔	CKEB0	[9]	
MDA9	AJ37	DDR0_DQ[9]	DDR0_CKE[0]	AW24	CKEA1	↔	CKEA1	[8]		MD89	AL35	DDR1_DQ[9]/DDR0_DQ[25]	DDR1_CKE[0]	AV29	CKEB1	↔	CKEB1	[9]	
MDA10	AL38	DDR0_DQ[10]	DDR0_CKE[1]	AW24	CKEA2	↔	CKEA2	[8]		MD810	AL32	DDR1_DQ[10]/DDR0_DQ[26]	DDR1_CKE[1]	AW29	CKEB2	↔	CKEB2	[9]	
MDA11	AL37	DDR0_DQ[11]	DDR0_CKE[2]	AV25	CKEA3	↔	CKEA3	[8]		MD811	AL32	DDR1_DQ[11]/DDR0_DQ[27]	DDR1_CKE[2]	AU29	CKEB3	↔	CKEB3	[9]	
MDA12	AJ40	DDR0_DQ[12]	DDR0_CKE[3]							MD812	AL34	DDR1_DQ[12]/DDR0_DQ[28]	DDR1_CKE[3]						
MDA13	AJ39	DDR0_DQ[13]		AW12	M_CSA0	↔	M_CSA0	[8]		MD813	AL34	DDR1_DQ[13]/DDR0_DQ[29]							
MDA14	AL39	DDR0_DQ[14]	DDR0_CS[0]	AU11	M_CSA1	↔	M_CSA1	[8]		MD814	AK31	DDR1_DQ[14]/DDR0_DQ[30]	DDR1_CS[0]	AP17	M_CSB0	↔	M_CSB0	[9]	
MDA15	AL40	DDR0_DQ[15]	DDR0_CS[1]	AV13	M_CSA2	↔	M_CSA2	[8]		MD815	AL31	DDR1_DQ[15]/DDR0_DQ[31]	DDR1_CS[1]	AN15	M_CSB1	↔	M_CSB1	[9]	
MDA16	AN38	DDR0_DQ[16]/DDR0_DQ[32]	DDR0_CS[2]	AV10	M_CSA3	↔	M_CSA3	[8]		MD816	AP36	DDR1_DQ[16]/DDR0_DQ[48]	DDR1_CS[2]	AN17	M_CSB2	↔	M_CSB2	[9]	
MDA17	AN40	DDR0_DQ[17]/DDR0_DQ[33]	DDR0_CS[3]							MD817	AN35	DDR1_DQ[17]/DDR0_DQ[49]	DDR1_CS[3]	AM15	M_CSB3	↔	M_CSB3	[9]	
MDA18	AR38	DDR0_DQ[18]/DDR0_DQ[34]		AW11	MODT_A0					MD818	AN32	DDR1_DQ[18]/DDR0_DQ[50]		AM16	MODT_B0				
MDA19	AR37	DDR0_DQ[19]/DDR0_DQ[35]	DDR0_ODT[0]	AU14	MODT_A1					MD820	AN34	DDR1_DQ[19]/DDR0_DQ[51]	DDR1_ODT[0]	AL16	MODT_B1				
MDA20	AN39	DDR0_DQ[20]/DDR0_DQ[36]	DDR0_ODT[1]	AU12	MODT_A2					MD821	AP34	DDR1_DQ[20]/DDR0_DQ[52]	DDR1_ODT[1]	AP15	MODT_B2				
MDA21	AN37	DDR0_DQ[21]/DDR0_DQ[37]	DDR0_ODT[2]	AY10	MODT_A3					MD822	AN31	DDR1_DQ[21]/DDR0_DQ[53]	DDR1_ODT[2]	AL15	MODT_B3				
MDA22	AR39	DDR0_DQ[22]/DDR0_DQ[38]	DDR0_ODT[3]							MD823	AP31	DDR1_DQ[22]/DDR0_DQ[54]	DDR1_ODT[3]						
MDA23	AR38	DDR0_DQ[23]/DDR0_DQ[39]		AY13	SBA00	↔	SBA00	[8]		MD824	AL29	DDR1_DQ[23]/DDR0_DQ[55]		AN18	MAAB16				
MDA24	AW37	DDR0_DQ[24]/DDR0_DQ[40]	DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	AV15	SBA01	↔	SBA01	[8]		MD825	AM29	DDR1_DQ[24]/DDR0_DQ[56]	DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]	AL17	MAAB16				
MDA25	AW38	DDR0_DQ[25]/DDR0_DQ[41]	DDR0_BA[1]/DDR0_CAB[5]/DDR0_BA[1]	AW23	BG_A0	↔	BG_A0	[8]		MD826	AP29	DDR1_DQ[25]/DDR0_DQ[57]	DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	AP16	MAAB15				
MDA26	AV35	DDR0_DQ[26]/DDR0_DQ[42]	DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]							MD827	AR29	DDR1_DQ[26]/DDR0_DQ[58]	DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]						
MDA27	AW35	DDR0_DQ[27]/DDR0_DQ[43]		AW15	MAAA16					MD828	AM28	DDR1_DQ[27]/DDR0_DQ[59]		AL18	SBA00	↔	SBA00	[9]	
MDA28	AU37	DDR0_DQ[28]/DDR0_DQ[44]	DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	AV14	MAAA14					MD829	AL28	DDR1_DQ[28]/DDR0_DQ[60]	DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]	AW28	SBAB1	↔	SBAB1	[9]	
MDA29	AV37	DDR0_DQ[29]/DDR0_DQ[45]	DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	AY11	MAAA15					MD830	AR28	DDR1_DQ[29]/DDR0_DQ[61]	DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]		SB_B0	↔	SB_B0	[9]	
MDA30	AT35	DDR0_DQ[30]/DDR0_DQ[46]	DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]							MD831	AP28	DDR1_DQ[30]/DDR0_DQ[62]							
MDA31	AU35	DDR0_DQ[31]/DDR0_DQ[47]		AW15	MAAA0					MD832	AR12	DDR1_DQ[31]/DDR0_DQ[63]		AL19	MAAB0				
MDA32	AY38	DDR0_DQ[32]/DDR1_DQ[0]	DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	AU18	MAAA1					MD833	AP12	DDR1_DQ[32]/DDR1_DQ[16]	DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]	AL22	MAAB1				
MDA33	AW38	DDR0_DQ[33]/DDR1_DQ[1]	DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	AU17	MAAA2					MD834	AM13	DDR1_DQ[33]/DDR1_DQ[17]	DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]	AM22	MAAB2				
MDA34	AV36	DDR0_DQ[34]/DDR1_DQ[2]	DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	MD835	AM13					MD835	AM13	DDR1_DQ[34]/DDR1_DQ[18]	DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]	AM23	MAAB3				
MDA35	AU6	DDR0_DQ[35]/DDR1_DQ[3]	DDR0_MA[3]	AT19	MAAA4					MD836	AR13	DDR1_DQ[35]/DDR1_DQ[19]	DDR1_MA[3]	AP23	MAAB4				
MDA36	AU8	DDR0_DQ[36]/DDR1_DQ[4]	DDR0_MA[4]	AU20	MAAA5					MD837	AP13	DDR1_DQ[36]/DDR1_DQ[20]	DDR1_MA[4]	AL23	MAAB5				
MDA37	AV8	DDR0_DQ[37]/DDR1_DQ[5]	DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	AV20	MAAA6					MD838	AM12	DDR1_DQ[37]/DDR1_DQ[21]	DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]	AW26	MAAB6				
MDA38	AW6	DDR0_DQ[38]/DDR1_DQ[6]	DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]	AU21	MAAA7					MD839	AL12	DDR1_DQ[38]/DDR1_DQ[22]	DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]	AU26	MAAB7				
MDA39	AY4	DDR0_DQ[39]/DDR1_DQ[7]	DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	AT20	MAAA8					MD840	AP10	DDR1_DQ[39]/DDR1_DQ[23]	DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]	AW26	MAAB8				
MDA40	AY4	DDR0_DQ[40]/DDR1_DQ[8]	DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]	AT22	MAAA9					MD841	AR10	DDR1_DQ[40]/DDR1_DQ[24]	DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]	AW27	MAAB9				
MDA41	AV4	DDR0_DQ[41]/DDR1_DQ[9]	DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	AY14	MAAA10					MD842	AR7	DDR1_DQ[41]/DDR1_DQ[25]	DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]	AP18	MAAB10				
MDA42	AT1	DDR0_DQ[42]/DDR1_DQ[10]	DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]	AU22	MAAA11					MD843	AP7	DDR1_DQ[42]/DDR1_DQ[26]	DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]	AV27	MAAB11				
MDA43	AT2	DDR0_DQ[43]/DDR1_DQ[11]	DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]	AV22	MAAA12					MD844	AR9	DDR1_DQ[43]/DDR1_DQ[27]	DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]	AU27	MAAB12				
MDA44	AV3	DDR0_DQ[44]/DDR1_DQ[12]	DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	AY24	MAAA13					MD845	AP9	DDR1_DQ[44]/DDR1_DQ[28]	DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]	AR15	MAAB13				
MDA45	AH1	DDR0_DQ[45]/DDR1_DQ[13]	DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]	AV23	BG_A1	↔	BG_A1	[8]		MD846	AR6	DDR1_DQ[45]/DDR1_DQ[29]	DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]	AG7	M_DQSB7				
MDA46	AT4	DDR0_DQ[46]/DDR1_DQ[14]	DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]	AU24		↔	M_ACT_A	[8]		MD847	AP6	DDR1_DQ[46]/DDR1_DQ[30]	DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]	AL28	SB_B1	↔	SB_B1	[9]	
MDA47	AT3	DDR0_DQ[47]/DDR1_DQ[15]	DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#							MD848	AM10	DDR1_DQ[47]/DDR1_DQ[31]	DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#	AL20	M_DDR_PARB	↔	M_DDR_PARB	[9]	
MDA48	AP2	DDR0_DQ[48]/DDR1_DQ[16]		AY15	DDR0_PAR	↔	M_ALERT_A	[8]		MD849	AL10	DDR1_DQ[48]		AY25	M_ALERT_B	↔	M_ALERT_B	[9]	
MDA49	AM4	DDR0_DQ[49]/DDR1_DQ[17]	DDR0_PAR	AT23		↔	M_ALERT_A	[8]		MD850	AM7	DDR1_DQ[49]	DDR1_PAR						
MDA50	AP3	DDR0_DQ[50]/DDR1_DQ[18]	DDR0_ALERT#							MD851	AL7	DDR1_DQ[50]	DDR1_ALERT#						
MDA51	AM3	DDR0_DQ[51]/DDR1_DQ[19]								MD852	AM9	DDR1_DQ[51]							
MDA52	AP4	DDR0_DQ[52]/DDR1_DQ[20]								MD853	AL9	DDR1_DQ[52]		AF34	M_DQSB0				
MDA53	AM2	DDR0_DQ[53]/DDR1_DQ[21]	DDR0_DQSN[0]	AF39	M_DQSA0					MD854	AM6	DDR1_DQ[53]	DDR1_DQSN[0]/DDR0_DQSN[2]	AK33	M_DQSB1				
MDA54	AP1	DDR0_DQ[54]/DDR1_DQ[22]	DDR0_DQSN[1]	AK39	M_DQSA1					MD855	AL6	DDR1_DQ[54]	DDR1_DQSN[1]/DDR0_DQSN[3]	AN33	M_DQSB2				
MDA55	AM1	DDR0_DQ[55]/DDR1_DQ[23]	DDR0_DQSN[2]/DDR0_DQSN[4]	AP39	M_DQSA2					MD856	AJ8	DDR1_DQ[55]	DDR1_DQSN[2]/DDR0_DQSN[6]	AN29	M_DQSB3				
MDA56	AK3	DDR0_DQ[56]/DDR1_DQ[24]	DDR0_DQSN[3]/DDR0_DQSN[5]	AU36	M_DQSA3					MD857	AE7	DDR1_DQ[56]	DDR1_DQSN[3]/DDR0_DQSN[7]	AN13	M_DQSB4				
MDA57	AH1	DDR0_DQ[57]/DDR1_DQ[25]	DDR0_DQSN[4]/DDR1_DQSN[0]	AW17	M_DQSA4					MD858	AE6	DDR1_DQ[57]	DDR1_DQSN[4]/DDR1_DQSN[2]	AR8	M_DQSB5				
MDA58	AK4	DDR0_DQ[58]/DDR1_DQ[26]	DDR0_DQSN[5]/DDR1_DQSN[1]	AU3	M_DQSA5					MD859	AE7	DDR1_DQ[58]	DDR1_DQSN[5]/DDR1_DQSN[3]	AM8	M_DQSB6				
MDA59	AH2	DDR0_DQ[59]/DDR1																	

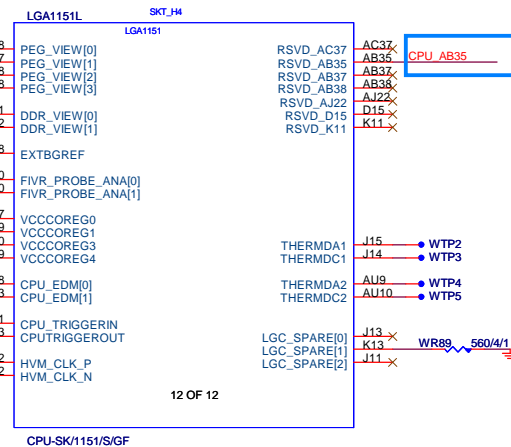
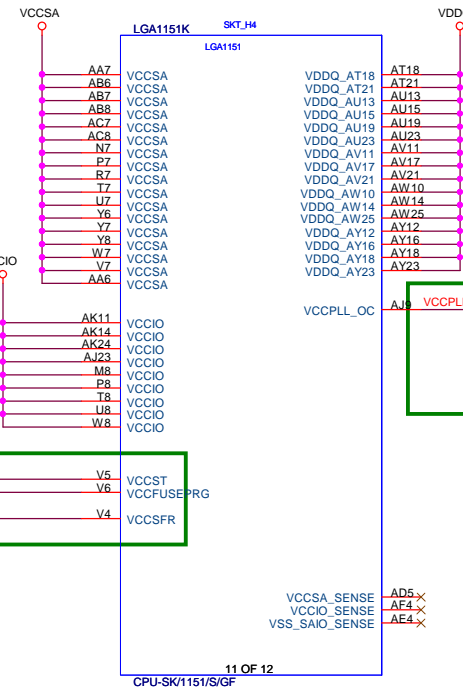
CFL\_R0.4

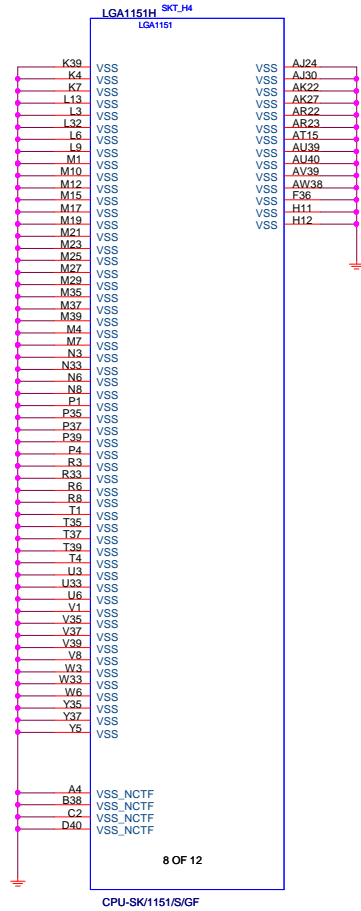
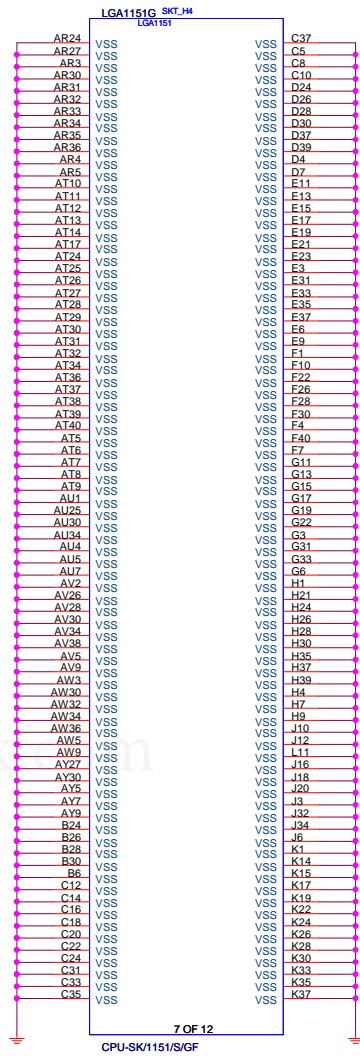
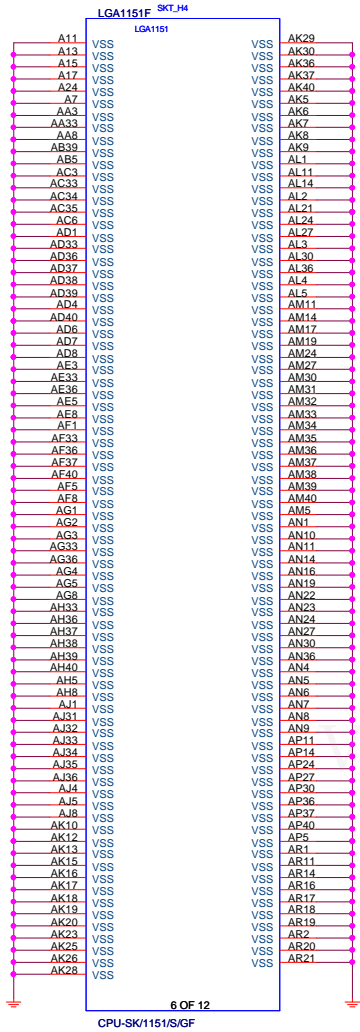
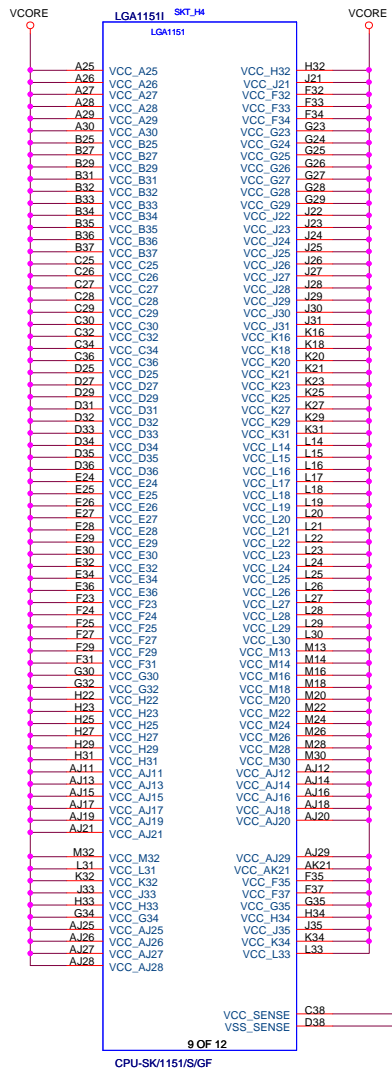


CPU POWER



CPU POWER

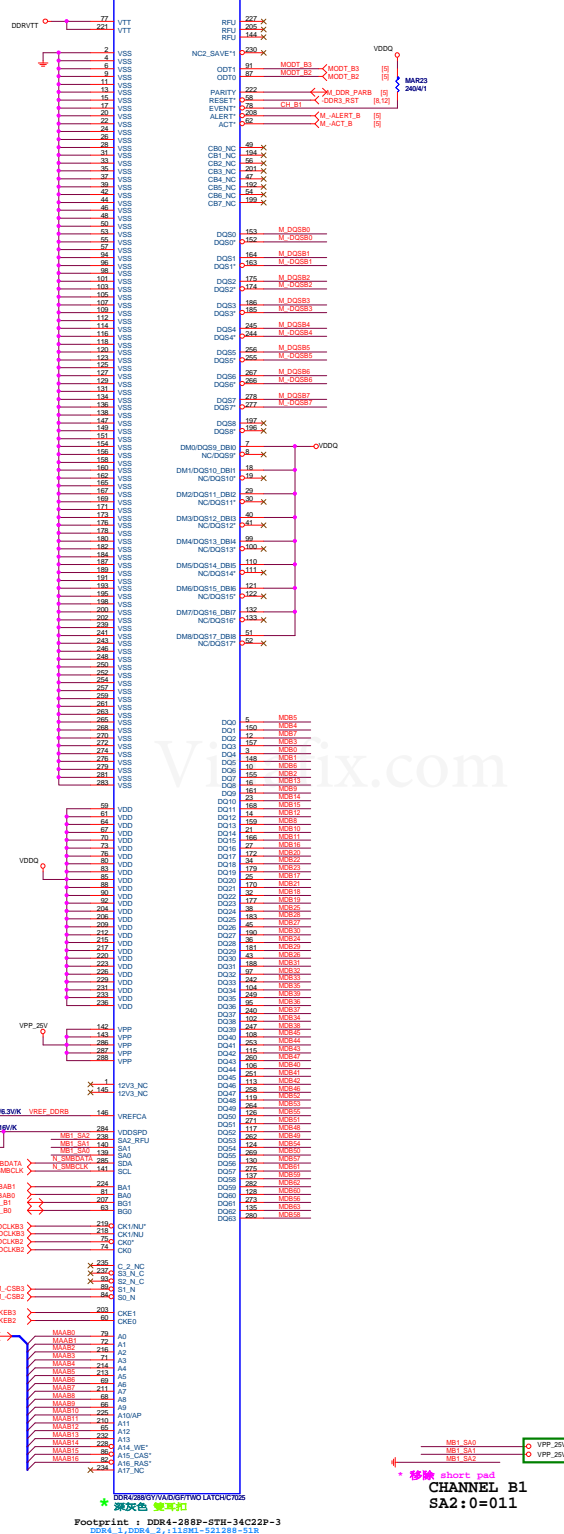


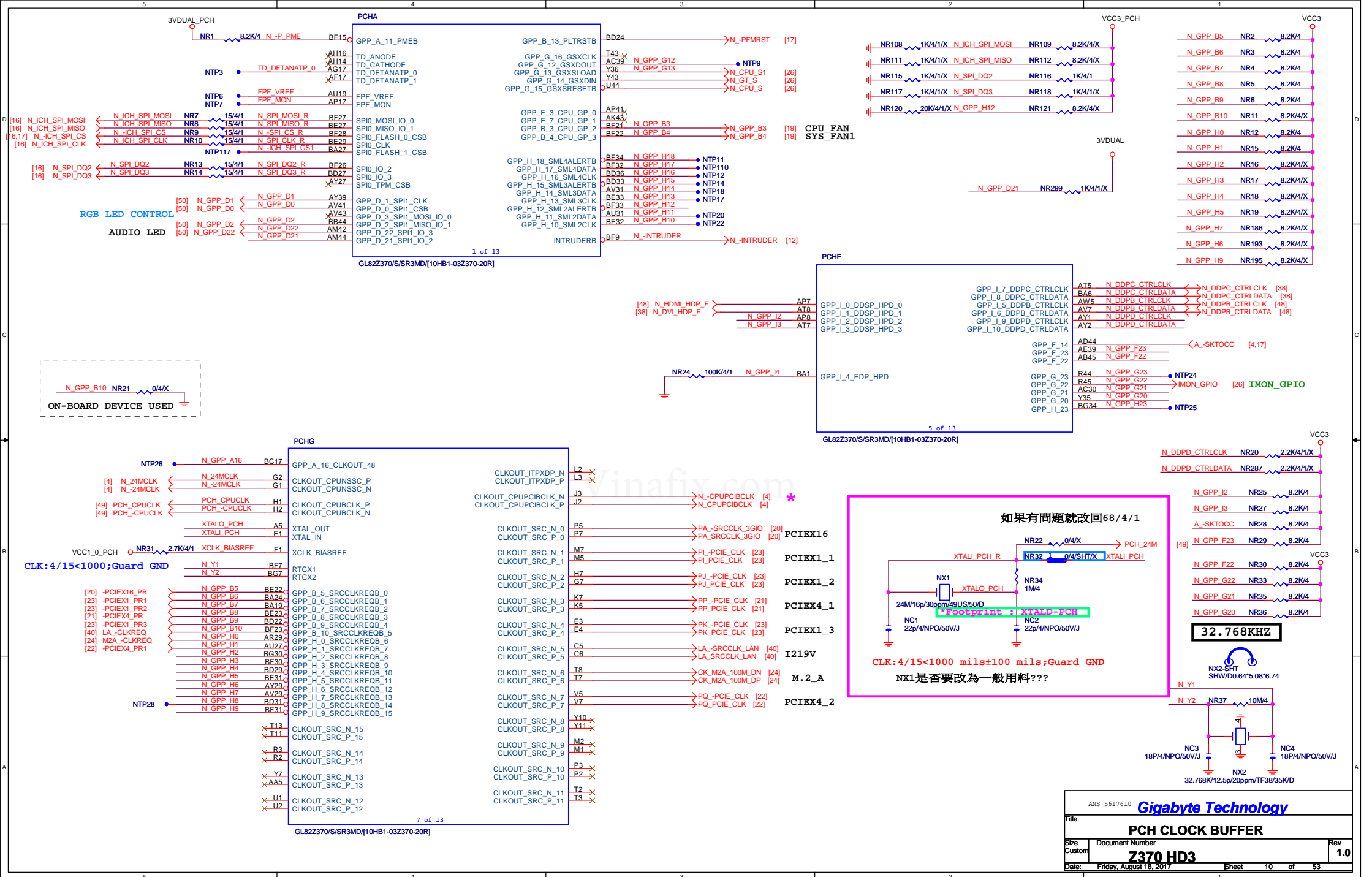


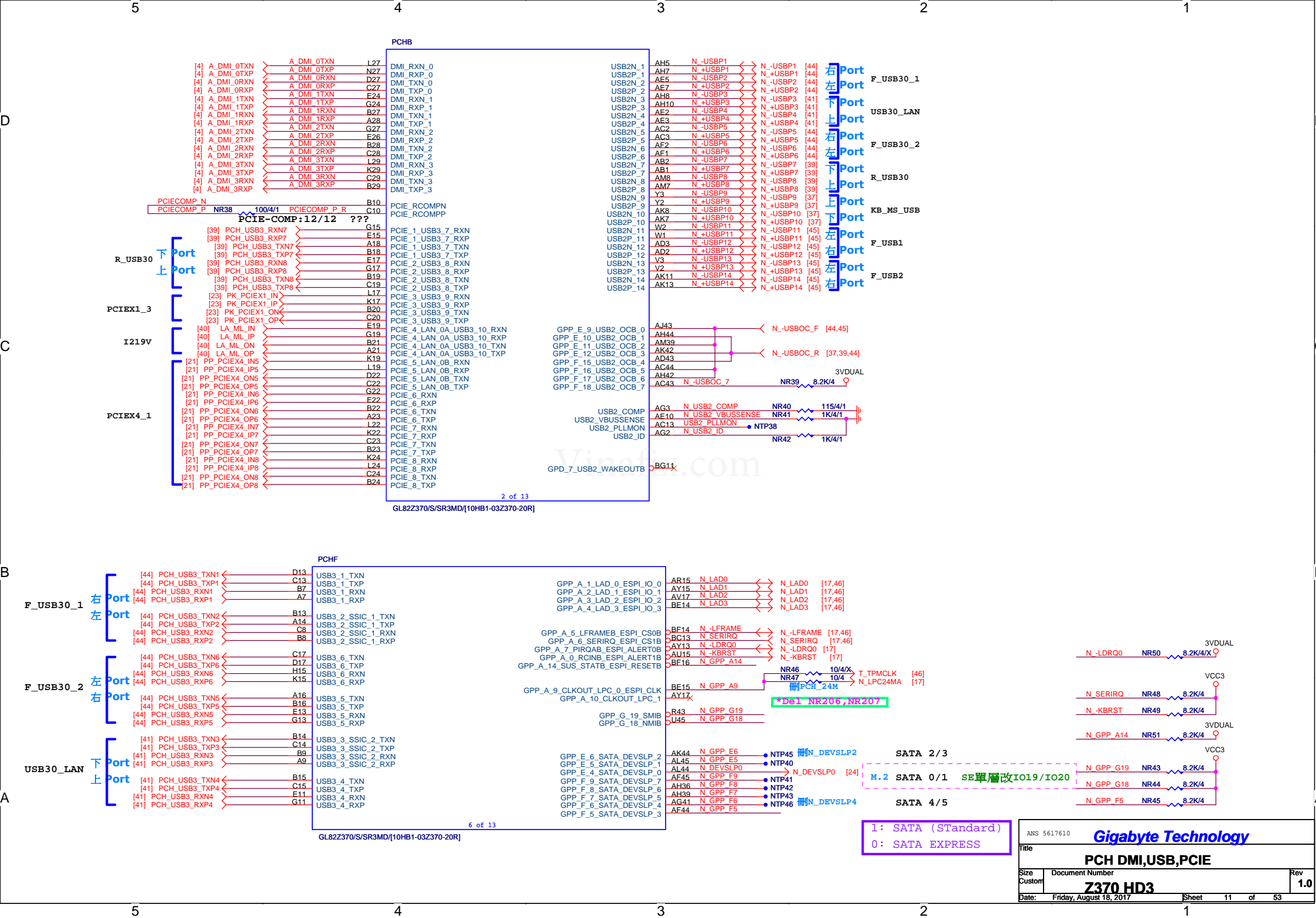


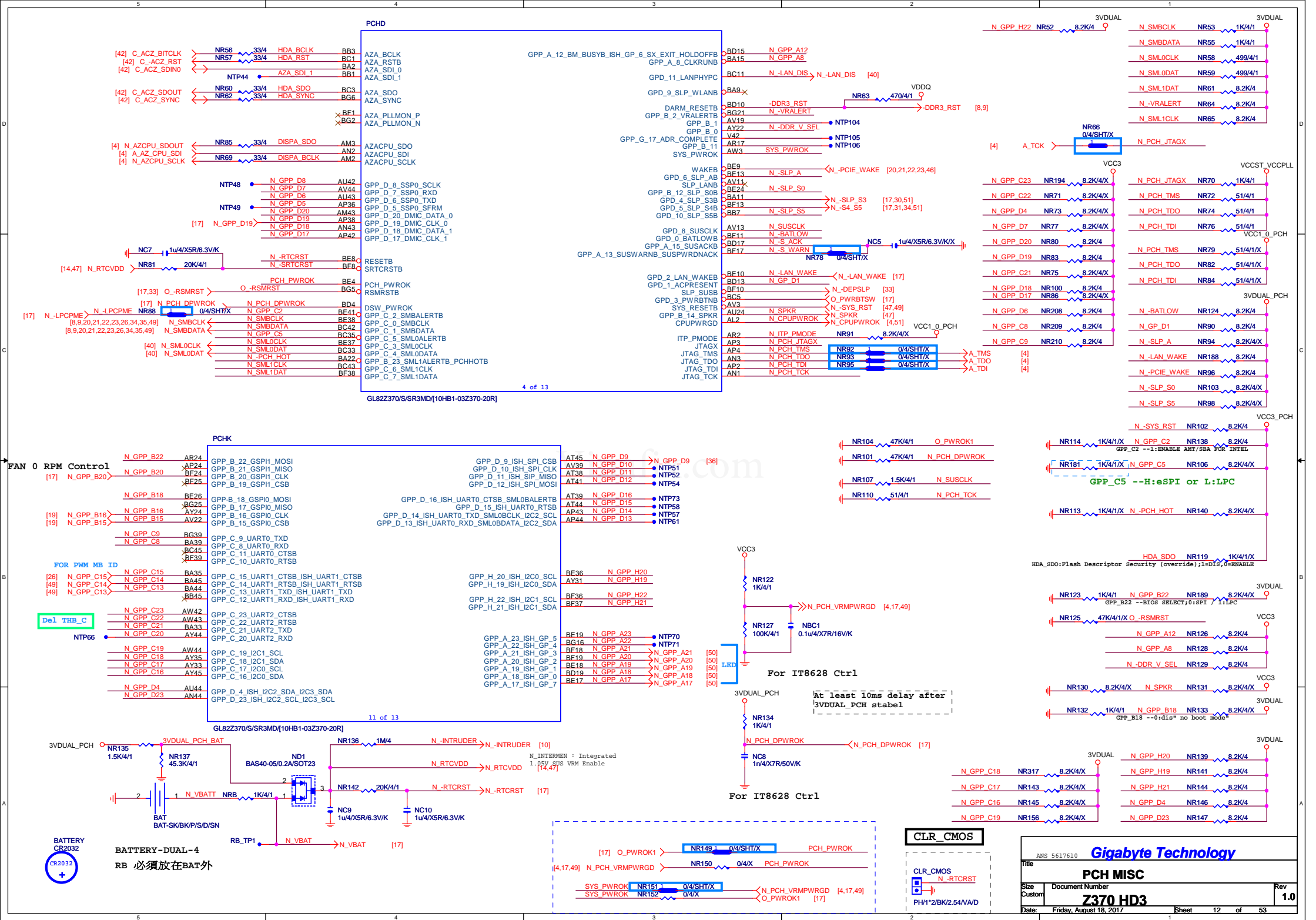


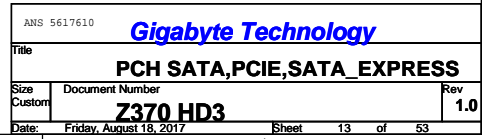
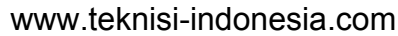




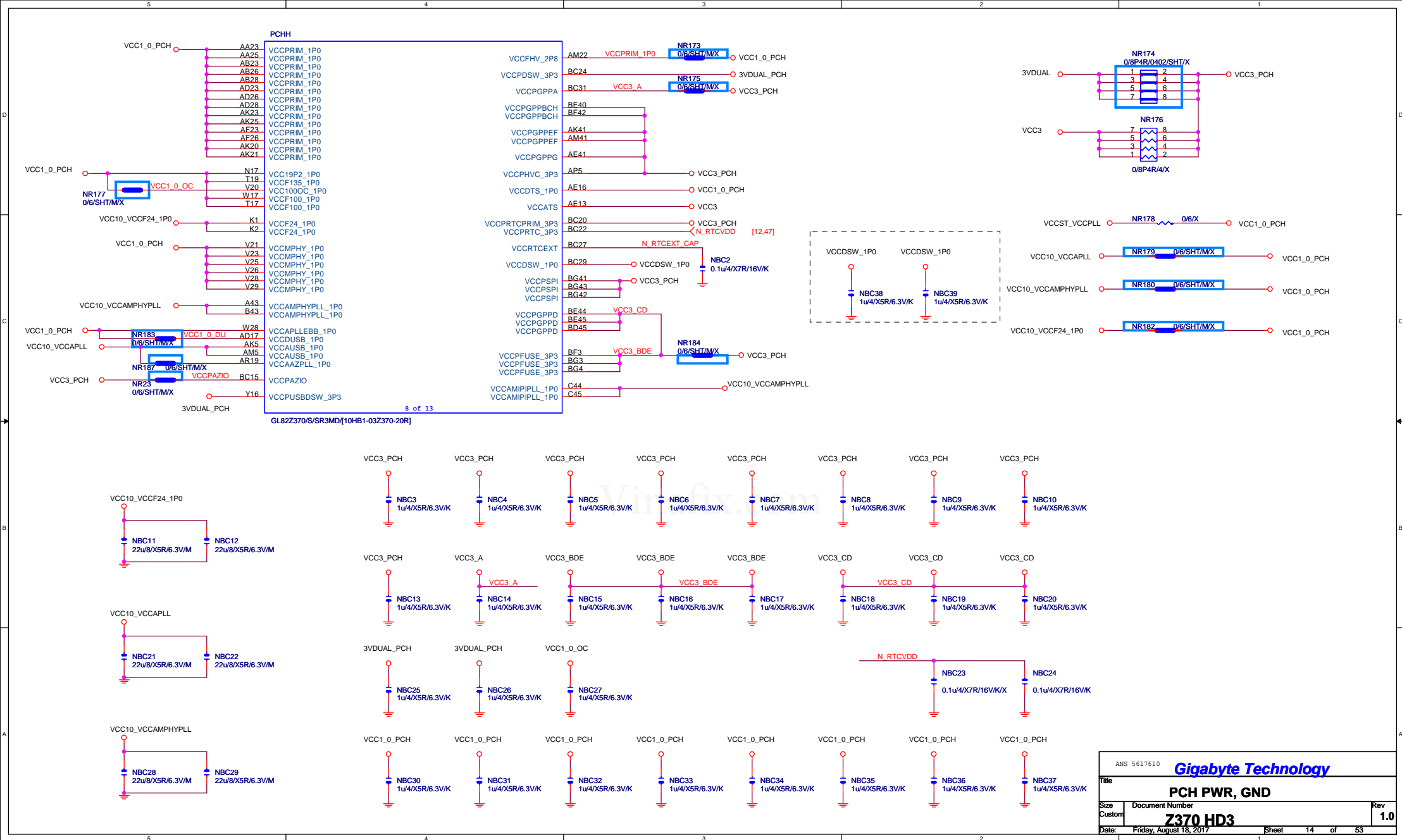






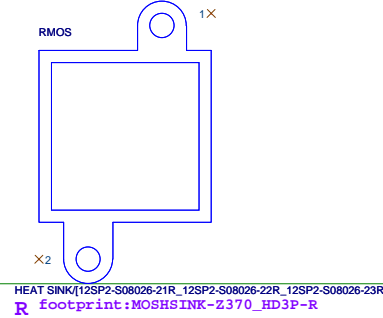
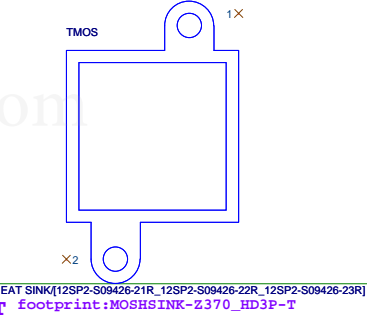
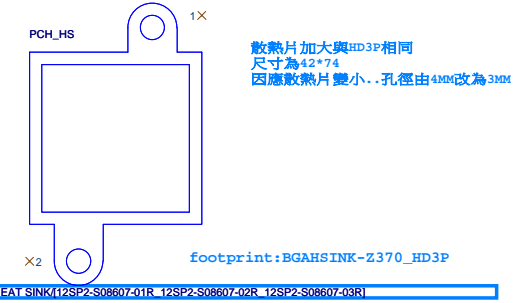






# 裝甲HEATSINK 分成四大部份

Location: PCH\_HS 12SP2-S08607-01R/02R/03R  
Location: TMOS 12SP2-S09426-21R/22R/23R  
Location: RMOS 12SP2-S08026-21R/22R/23R



- \* PCB顏色 : 咖啡黑(咖啡)
- \* 文字面 : 灰色
- \* 圖騰 : 灰色斜線圖騰A

刪AUDIO\_HS

Footprint :  
X99-ARMOR-AUDIO

刪REAR\_ARMOR

Footprint :  
REAR\_ARMOR-Z270X-GAMING7

刪REAR\_HS

鐵件裝甲  
Footprint :  
Z270X-GAMING7\_ARMOR

塑膠裝甲

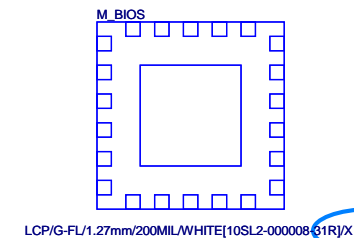
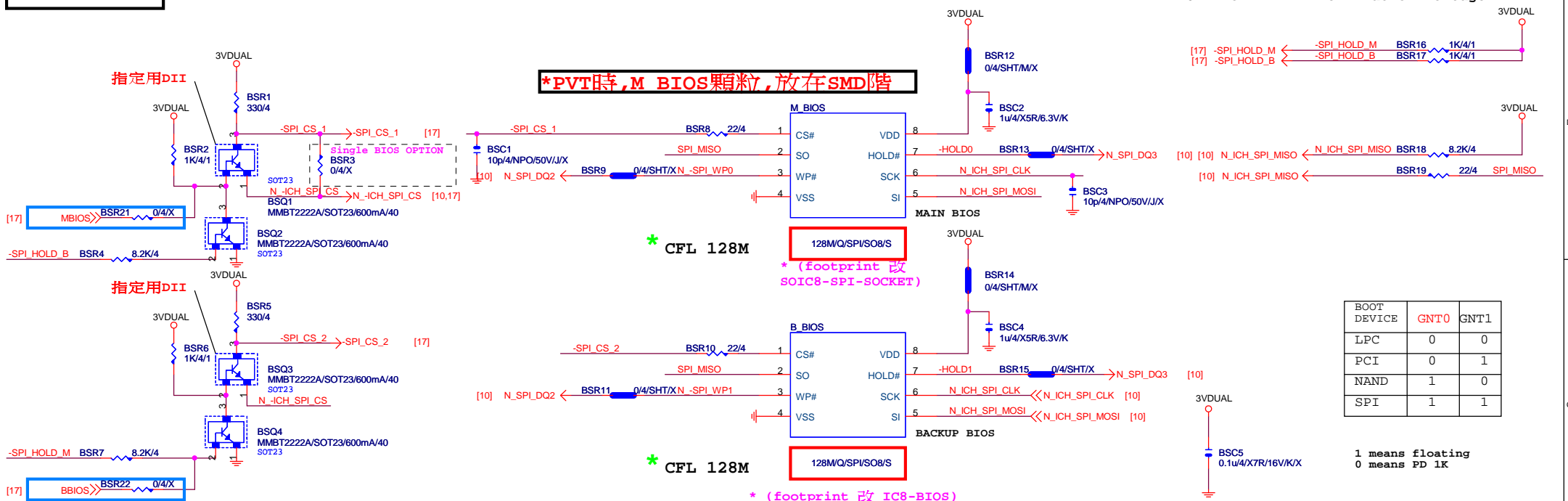
ANSI 5617610 <b>Gigabyte Technology</b>			
Title <b>PCH PWR, GND</b>			
Size Custom	Document Number <b>Z370 HD3</b>		Rev <b>1.0</b>
Date: Friday, August 18, 2017	Sheet 15	of 53	

PCHI		
A25	VSS	A42
A30	VSS	D45
P22	VSS	BG44
AV38	VSS	BF44
AV45	VSS	BF45
AV8	VSS	BF2
AV11	VSS	W29
AV19	VSS	A35
AY37	VSS	A40
AY4	VSS	A41
AY42	VSS	AA17
AY8	VSS	AA18
B25	VSS	AA20
B3	VSS	AA21
B30	VSS	AA26
B35	VSS	AA28
B4	VSS	AA29
B41	VSS	AB17
BA13	VSS	AC32
BA17	VSS	AE
BA29	VSS	C9
BA31	VSS	AE4
BA37	VSS	AE8
BA4	VSS	AE18
BA42	VSS	AF20
BB40	VSS	AF21
BC38	VSS	AF25
BC40	VSS	AF28
BC9	VSS	AF29
BD11	VSS	AF4
BD16	VSS	AF42
BD2	VSS	AG18
BD21	VSS	AG20
BD25	VSS	AG21
F2	VSS	AG23
F31	VSS	AG25
E6	VSS	AG26
E8	VSS	AG28
F38	VSS	AG29
F43	VSS	AH11
G4	VSS	AH13
G40	VSS	AH30
G42	VSS	AH32
F6	VSS	AH33
G9	VSS	AH38
H11	VSS	AJ1
H13	VSS	AJ17
H17	VSS	AJ18
H19	VSS	AJ20
H22	VSS	AJ21
H24	VSS	AJ23
H27	VSS	AJ25
H29	VSS	AJ26
H33	VSS	AJ28
H35	VSS	AJ29
H38	VSS	AJ45
H4	VSS	AK10
H42	VSS	AK14
H9	VSS	AK16
J4	VSS	AK17
M36	VSS	AK18
M38	VSS	AK26
M4	VSS	AK28
M8	VSS	AM14
M9	VSS	AN14
N13	VSS	AP19
N15	VSS	AR22
N19	VSS	AR27
N22	VSS	AU29
N24	VSS	AU33
N31	VSS	AV1
N42	VSS	AV10
P10	VSS	AV15
P12	VSS	AV24
AV35	VSS	AV27
9 of 13		
GL822370/S/SR3MD[10HB1-03Z370-20R]		

PCHL		
BD34	VSS[70]	BD39
BD7	VSS[71]	BD7
BE2	VSS[72]	BE2
BF43	VSS[73]	BF43
BF5	VSS[74]	BF5
BG18	VSS[75]	BG18
BG23	VSS[76]	BG23
BG28	VSS[77]	BG28
BG32	VSS[78]	BG32
BG37	VSS[79]	BG37
BG40	VSS[80]	BG40
CG9	VSS[81]	CG9
C1	VSS[83]	C1
A12	VSS[84]	A12
C37	VSS[85]	C37
A6	VSS[86]	A6
C9	VSS[87]	C9
D1	VSS[88]	D1
D10	VSS[89]	D10
D12	VSS[90]	D12
D15	VSS[91]	D15
D16	VSS[92]	D16
R12	VSS[93]	R12
D19	VSS[94]	D19
D21	VSS[95]	D21
D24	VSS[96]	D24
D25	VSS[97]	D25
D29	VSS[98]	D29
AG20	VSS[99]	AG20
D30	VSS[100]	D30
D33	VSS[101]	D33
D35	VSS[102]	D35
D36	VSS[103]	D36
D32	VSS[104]	D32
D44	VSS[105]	D44
D7	VSS[106]	D7
P13	VSS[107]	P13
P15	VSS[108]	P15
P17	VSS[109]	P17
P19	VSS[110]	P19
P31	VSS[111]	P31
P33	VSS[112]	P33
P35	VSS[113]	P35
P4	VSS[114]	P4
P42	VSS[115]	P42
P8	VSS[116]	P8
R1	VSS[117]	R1
R32	VSS[118]	R32
T10	VSS[119]	T10
T14	VSS[120]	T14
T22	VSS[121]	T22
T29	VSS[122]	T29
T32	VSS[123]	T32
T36	VSS[124]	T36
T38	VSS[125]	T38
Y38	VSS[126]	Y38
Y4	VSS[127]	Y4
Y8	VSS[128]	Y8
T42	VSS[129]	T42
T5	VSS[130]	T5
U4	VSS[131]	U4
U42	VSS[132]	U42
V10	VSS[133]	V10
V14	VSS[134]	V14
W3	VSS[135]	W3
AR13	VSS[136]	AR13
AR31	VSS[137]	AR31
AR33	VSS[138]	AR33
AT42	VSS[139]	AT42
AU11	VSS[140]	AU11
AU17	VSS[141]	AU17
BD30	VSS[142]	BD30
W45	VSS[143]	W45
Y13	VSS[144]	Y13
Y14	VSS[145]	Y14
Y15	VSS[146]	Y15
Y16	VSS[147]	Y16
Y30	VSS[148]	Y30
Y32	VSS[149]	Y32
Y33	VSS[150]	Y33
BG14	VSS[151]	BG14
VSS_BG14	VSS[152]	VSS_BG14
12 of 13		
GL822370/S/SR3MD[10HB1-03Z370-20R]		

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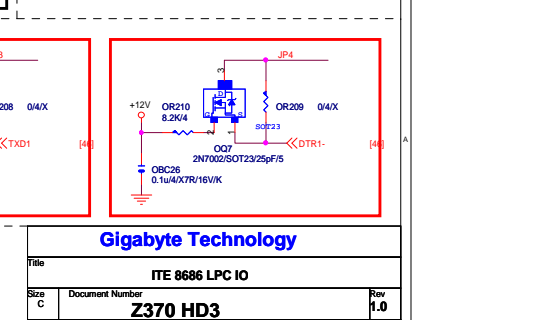
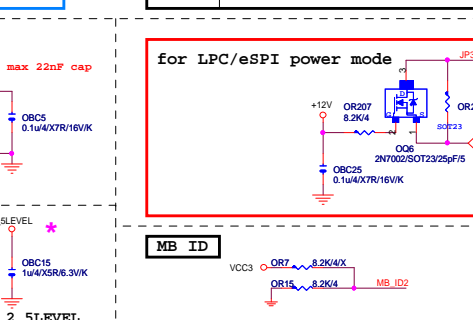
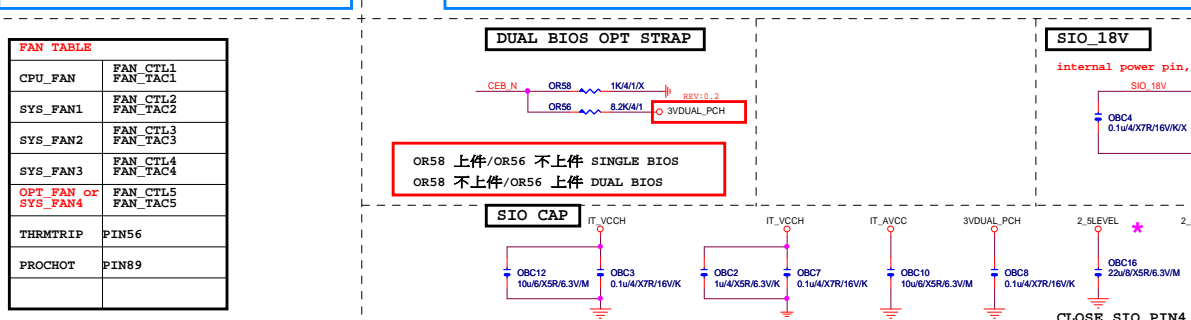




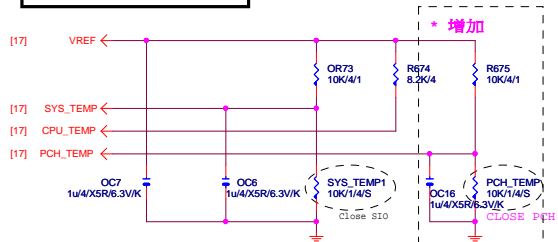
\* 試產先上, PVT 移除

**Gigabyte Technology**

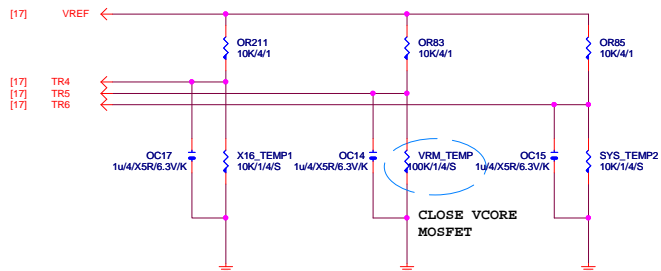
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Size	Document Number	Rev	
Custom	2370 HD3	1.0	
Date:	Tuesday, August 15, 2017	Sheet	16 of 53



# TEMP H/W MONITOR Rev0.5

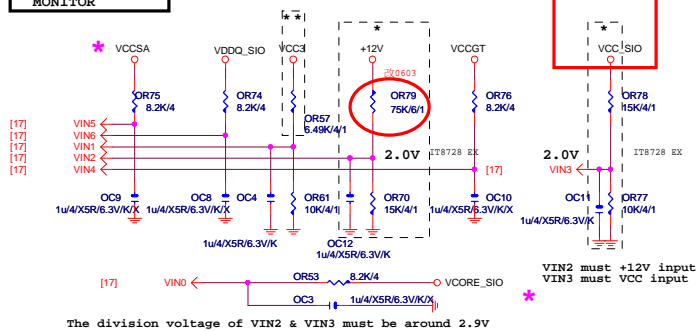


## 5個FAN時使用

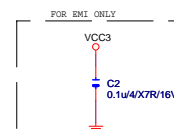
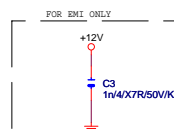


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# VOLTAGE-- H/W MONITOR



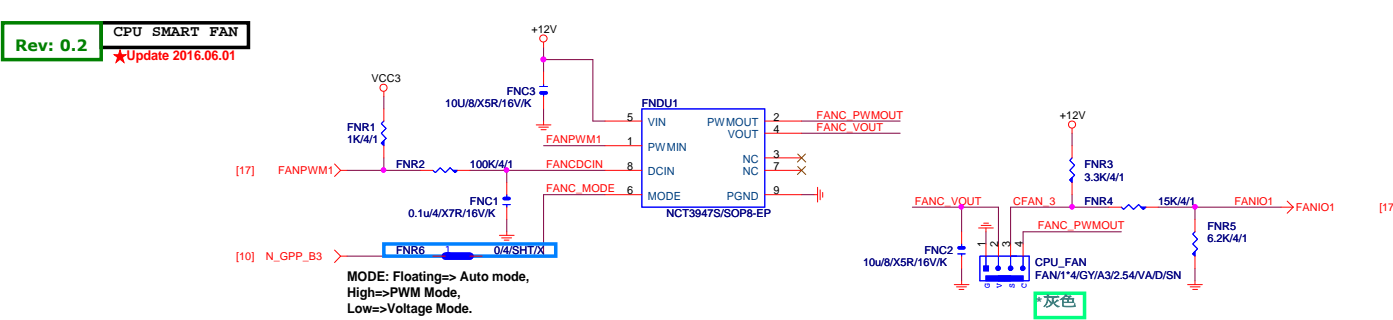
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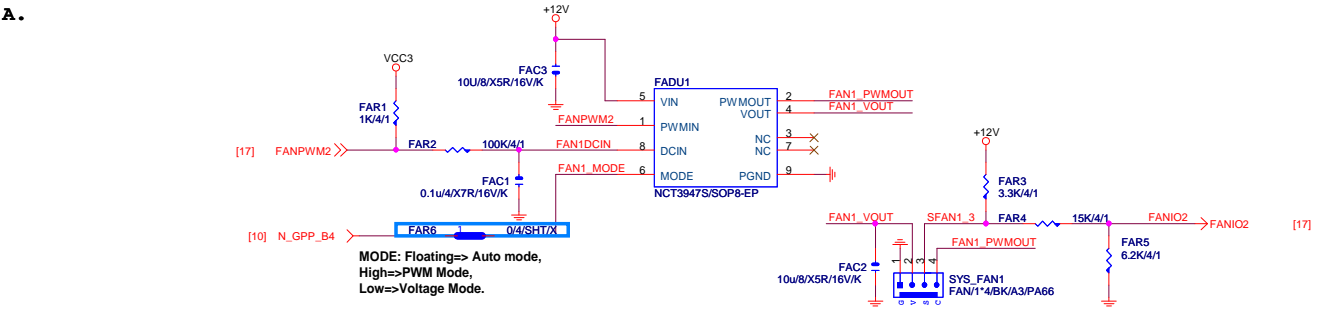
★Update 2015-04-24

Gigabyte Technology

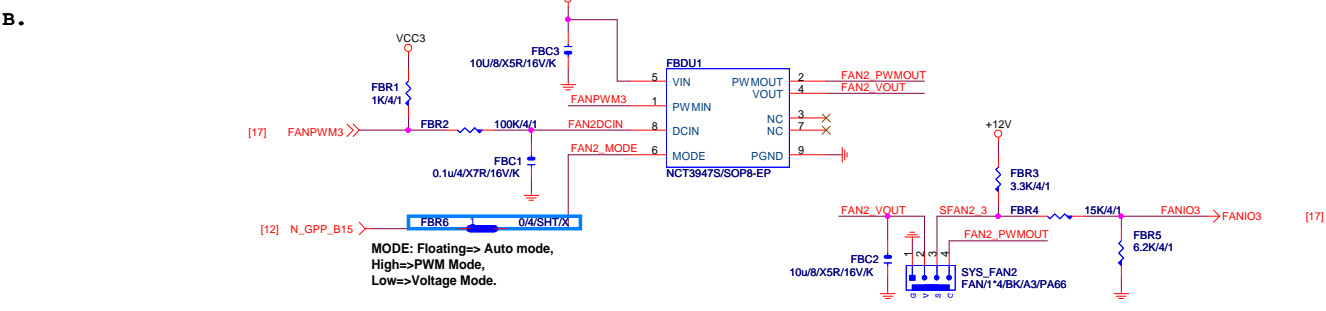
Title			HWM,KB/MS, FAN CTRL
Size	Document Number	Rev	
Custom	Z370 HD3	1.0	
Date:	Friday, July 28, 2017	Sheet	18 of 53



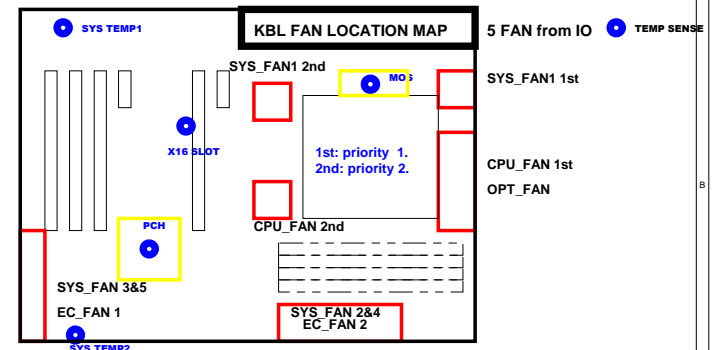
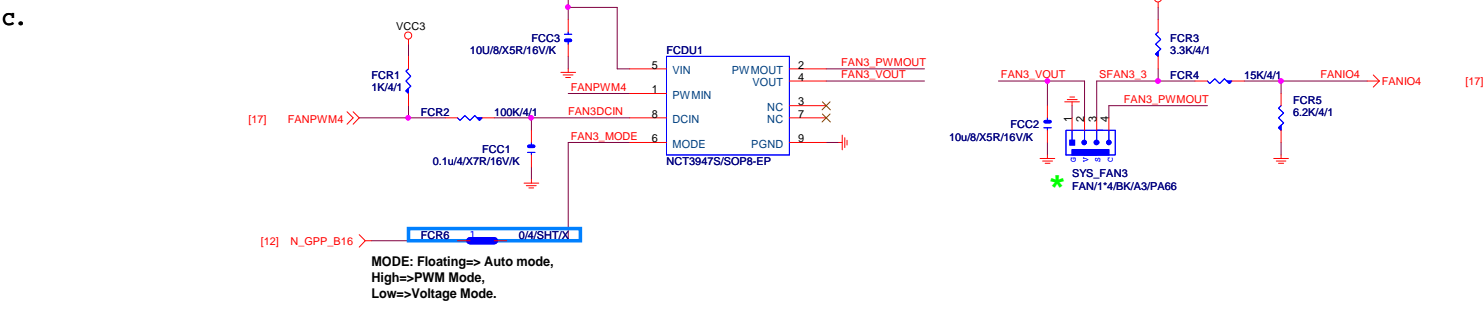
SYSTEM FAN1



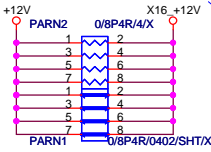
SYSTEM FAN2



SYSTEM FAN3



Rev 0.2

+12V - protect  
short-wire test

Footprint : PCIESLOT-164STH

3GIO\_\*16

[8,9,12,21,22,23,26,34,35,49] N\_SMBCLK  
[8,9,12,21,22,23,26,34,35,49] N\_SMBDATA

[12,21,22,23,46] N\_-PCIE\_WAKE

[10] -PCIE16\_PR

PA\_EXP\_RXP[0..15] >> PA\_EXP\_RXP[0..15] [4]  
 PA\_EXP\_RXN[0..15] >> PA\_EXP\_RXN[0..15] [4]  
 PA\_EXP\_TXP[0..15] >> PA\_EXP\_TXP[0..15] [4]  
 PA\_EXP\_TXN[0..15] >> PA\_EXP\_TXN[0..15] [4]

PA_EXP_TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA_EXP_TXP0 C
PA_EXP_TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA_EXP_TXN0 C
PA_EXP_TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA_EXP_TXP1 C
PA_EXP_TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA_EXP_TXN1 C
PA_EXP_TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA_EXP_TXP2 C
PA_EXP_TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA_EXP_TXN2 C
PA_EXP_TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA_EXP_TXP3 C
PA_EXP_TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA_EXP_TXN3 C
PA_EXP_TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA_EXP_TXP4 C
PA_EXP_TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA_EXP_TXN4 C
PA_EXP_TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA_EXP_TXP5 C
PA_EXP_TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA_EXP_TXN5 C
PA_EXP_TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA_EXP_TXP6 C
PA_EXP_TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA_EXP_TXN6 C
PA_EXP_TXP7	PAC18	0.22u/4/X5R/6.3V/K	PA_EXP_TXP7 C
PA_EXP_TXN7	PAC19	0.22u/4/X5R/6.3V/K	PA_EXP_TXN7 C
PA_EXP_TXP8	PAC20	0.22u/4/X5R/6.3V/K	PA_EXP_TXP8 C
PA_EXP_TXN8	PAC21	0.22u/4/X5R/6.3V/K	PA_EXP_TXN8 C
PA_EXP_TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA_EXP_TXP9 C
PA_EXP_TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA_EXP_TXN9 C
PA_EXP_TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA_EXP_TXP10 C
PA_EXP_TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA_EXP_TXN10 C
PA_EXP_TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA_EXP_TXP11 C
PA_EXP_TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA_EXP_TXN11 C
PA_EXP_TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA_EXP_TXP12 C
PA_EXP_TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA_EXP_TXN12 C
PA_EXP_TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA_EXP_TXP13 C
PA_EXP_TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA_EXP_TXN13 C
PA_EXP_TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA_EXP_TXP14 C
PA_EXP_TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA_EXP_TXN14 C
PA_EXP_TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA_EXP_TXP15 C
PA_EXP_TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA_EXP_TXN15 C

PCIE16:16/5/5/5/16

PCI-E REV:1.1--&gt; 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--&gt; 5GHZ

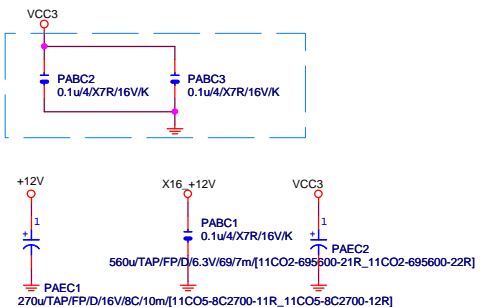
PCE-E X1(單向) BANDWIDTH=5GHz\*(8b/10b)=4Gb/s=500MB/s

PCI-E REV:3.0--&gt; 8GHZ

PCE-E X1(單向) BANDWIDTH=8GHz\*(128b/130b)=8Gb/s=1GB/s

PCIE16:164P/GYLONG DOUBLE/HK\*2

深灰色 (預留金屬加強,不上)

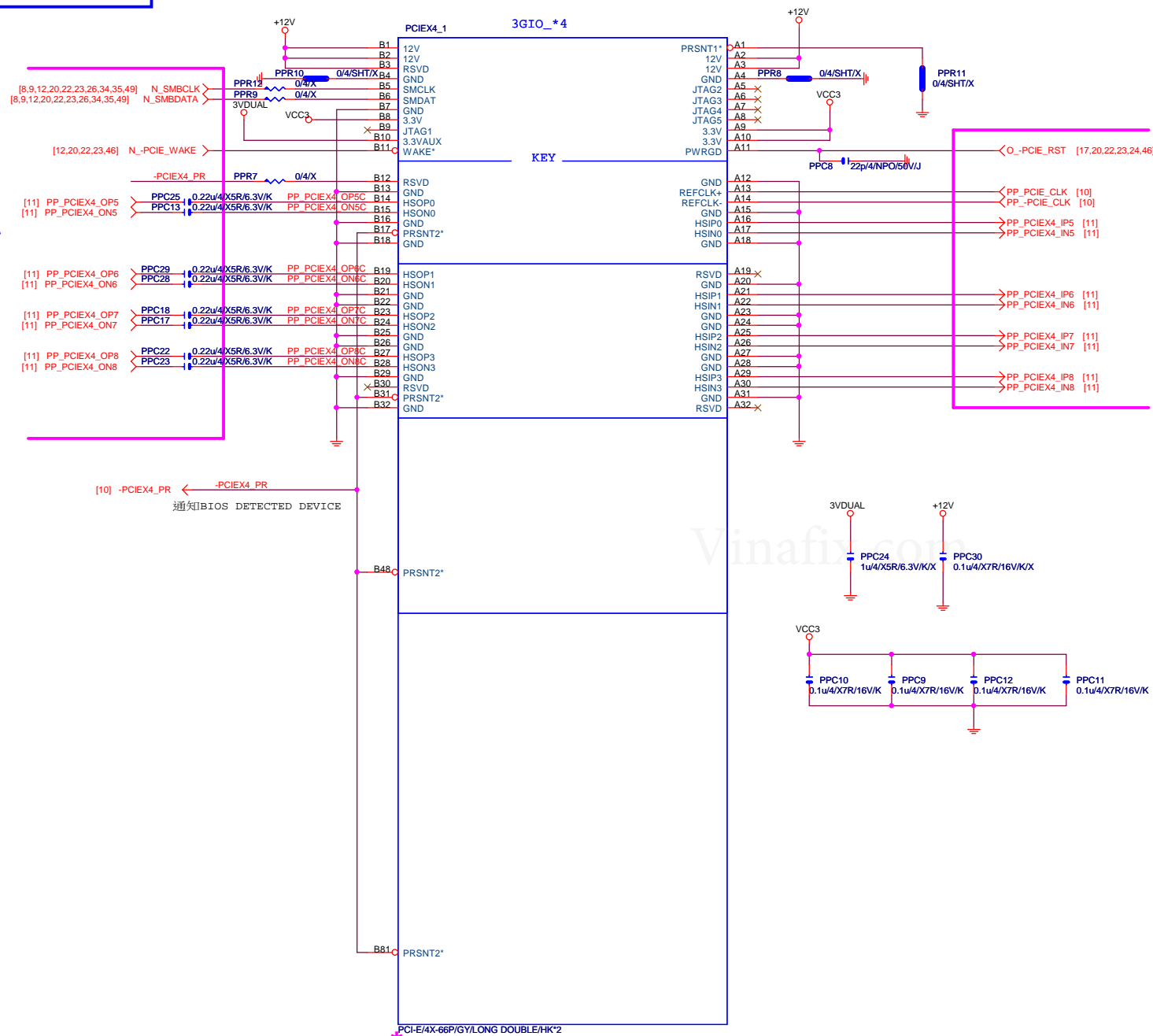


Gigabyte Technology		
PCI EXPRESS * 16		
Title	Document Number	Rev 1.0
Size Custom	Z370 HD3	
Date: Friday, July 28, 2017	Sheet 20	of 53

Rev 0.51

PCIE\*4

Footprint "PCIESLOT-64STH-1"



深灰色 (預留金屬加強, 不上)

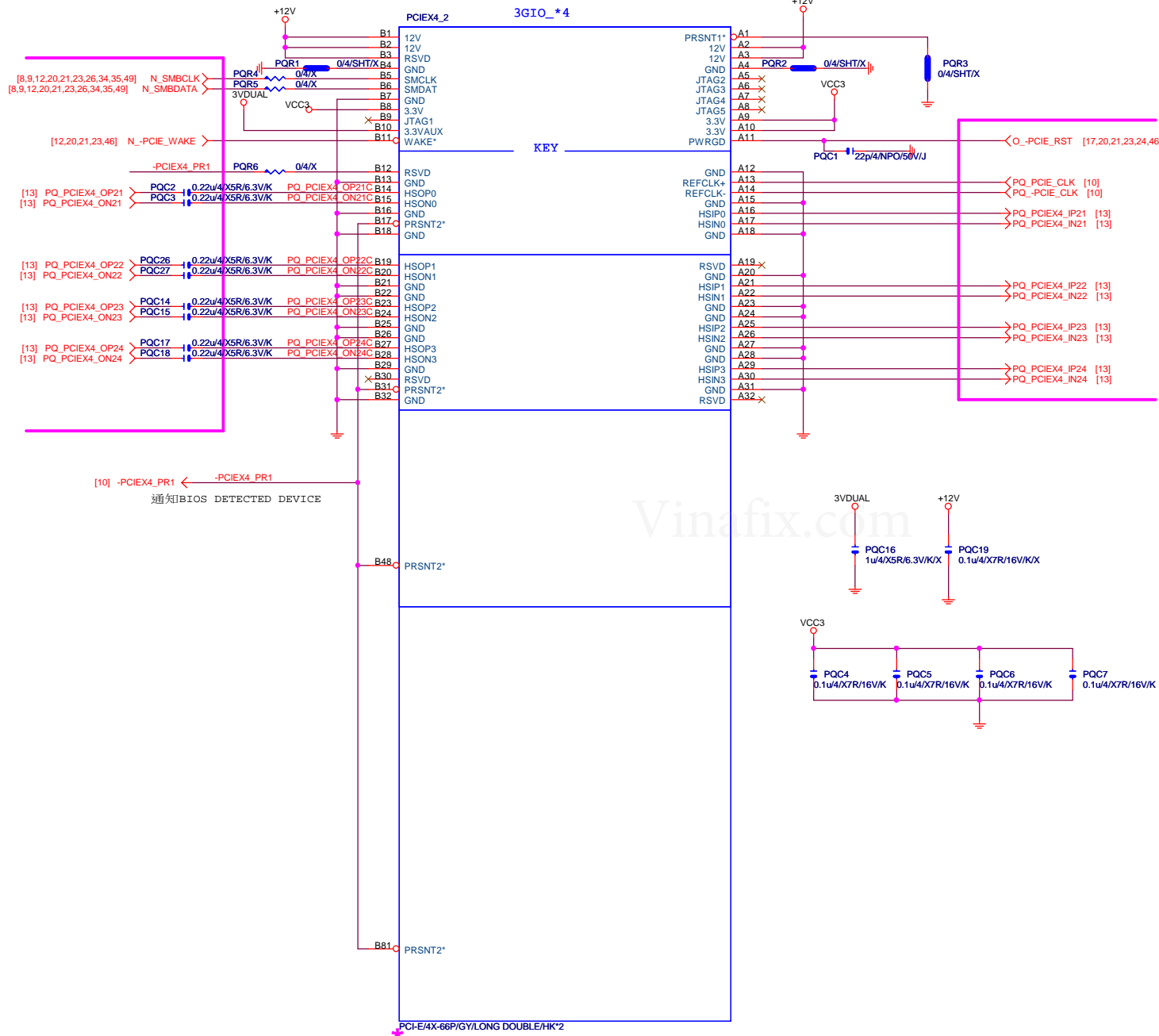
GIGABYTE™

Title		
ASM1142 & ASM2142 co-lay		
Size	Document Number	Rev
Custom	Z370 HD3	1.0
Date:	Friday, July 28, 2017	Sheet 21 of 53

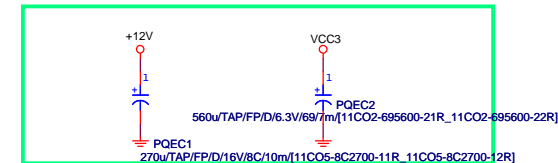
Rev 0.51

PCIE\*4

Footprint "PCIESLOT-64P-1"



Add PQEC1, PQEC2

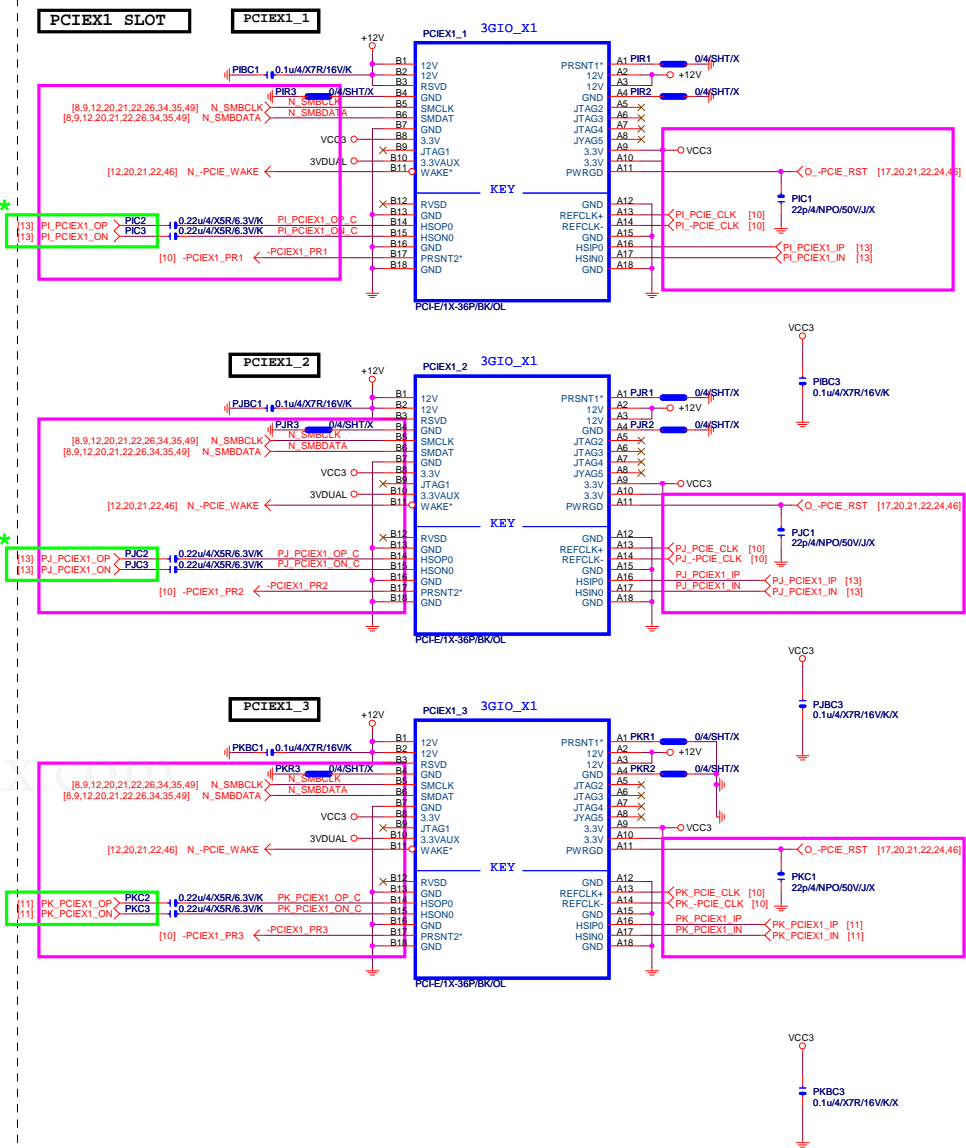


深灰色 (不留金屬加強,也不上)

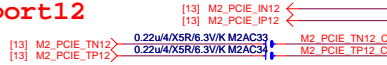
Gigabyte Technology			
Title	PCIE_X4		
Size	Document Number	Rev	
Custom	Z370 HD3	1.0	
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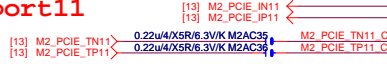
3個x1 ,不用SWITCH



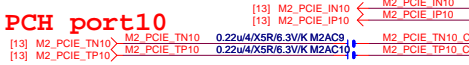
## M.2 Lane3 from PCH port12



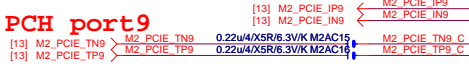
## M.2 Lane2 from PCH port11



## M.2 Lane1 from PCH port10

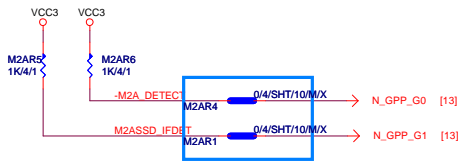


## M.2 Lane0 from PCH port9



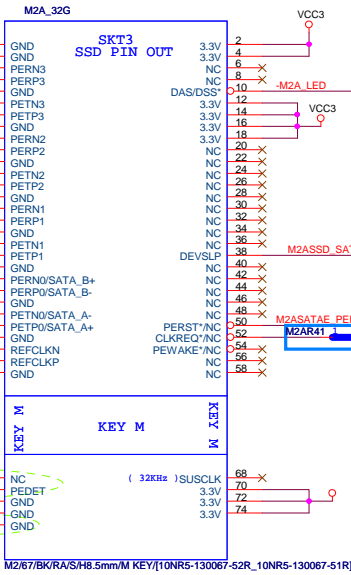
需與M2\_-CLKREQ對應

## 支援SATA and M.2 function



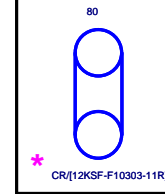
Footprint : NGFF-M-75P-11CM-3-SMD

M.2 有插卡 /沒插卡 GPP_G0	M.2插何種卡? GPP_G1	SATA Express 插何種硬碟? GPP_E0/E2/F1	IO15 (S0)	IO16 (S1)	IO17	IO18	IO19 (S0)	IP20 (S1)
有插卡 (Low)	SATA Mode (Low)	SATA (Hi)	SATA (M.2)	PCIE x1	PCIE x1	PCIE x1	PCIE x1	SATA
		SATA Express (Low)	SATA (M.2)	PCIE x1	PCIE x1	PCIE x1	SATA Express	
	PCIE Mode (Hi)	SATA (Hi)		PCIE x4 (For M.2)			SATA	SATA
		SATA Express (Low)		PCIE x4 (For M.2)			SATA Express	
沒插卡 (Hi)	Don't Care (Hi)	SATA (Hi)		PCIE x4			SATA	SATA
		SATA Express (Low)		PCIE x4			SATA Express	



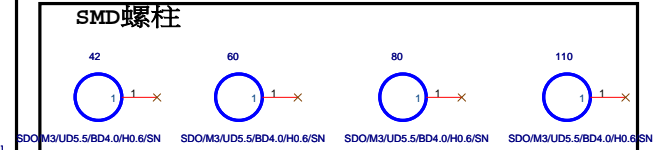
VCC3

## DIP螺柱

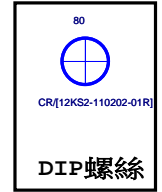


加高

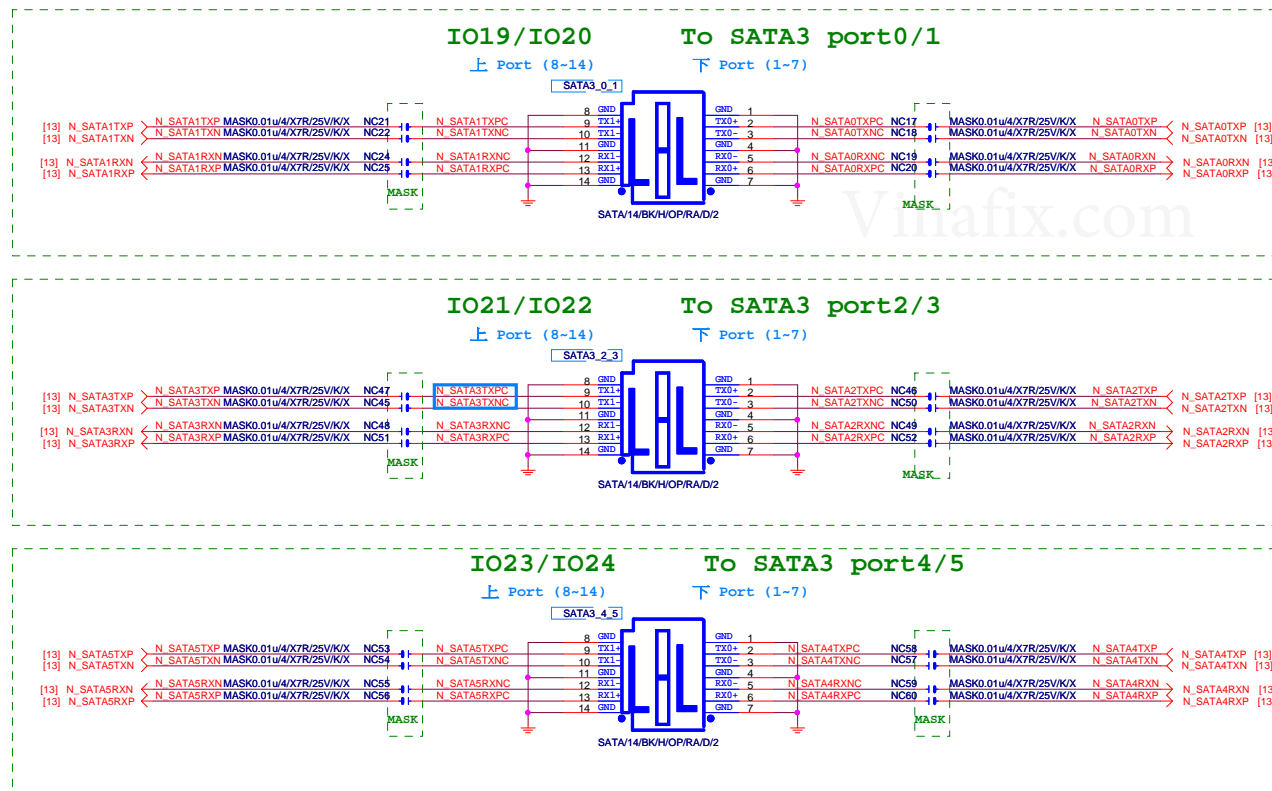
## SMD螺柱



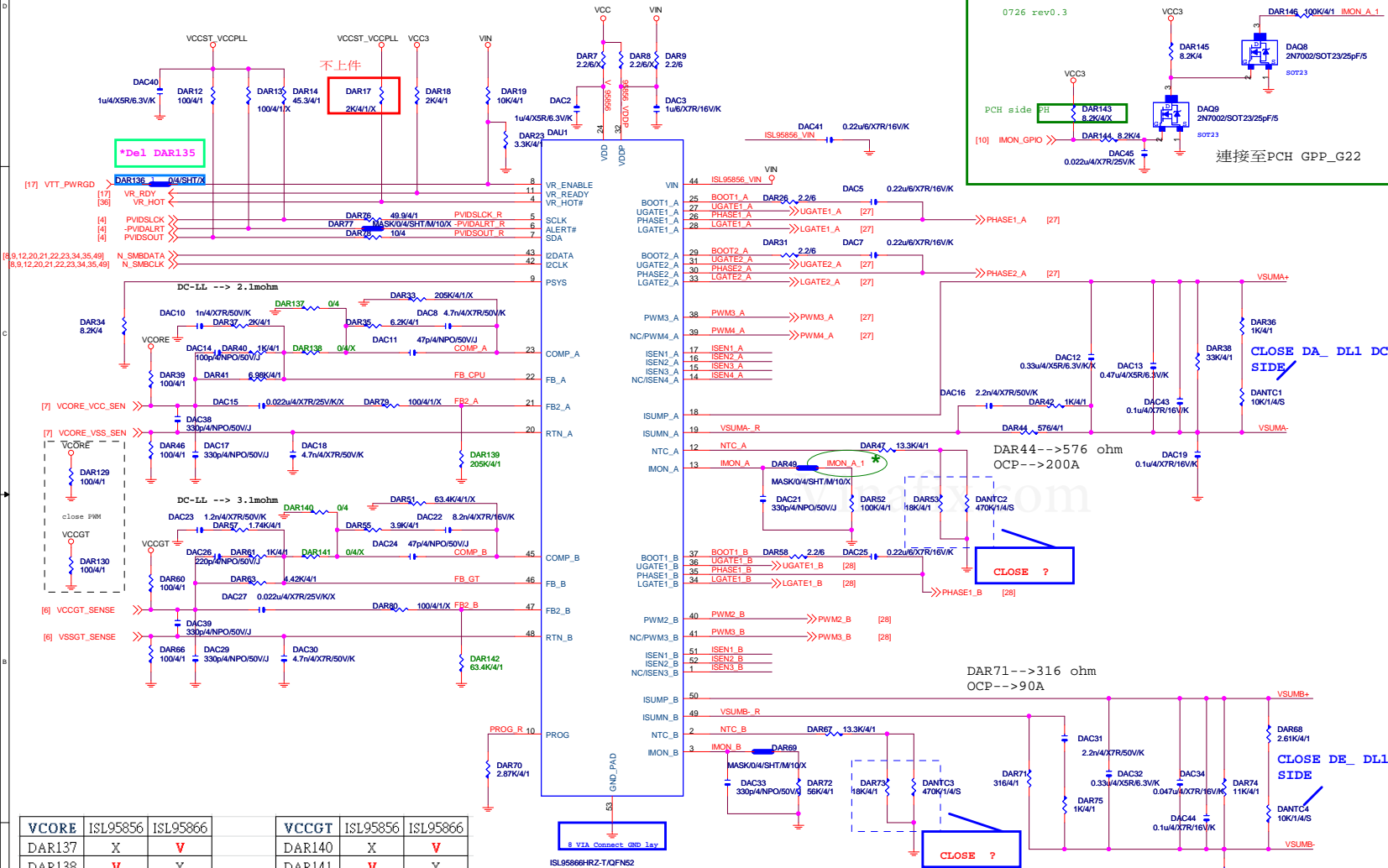
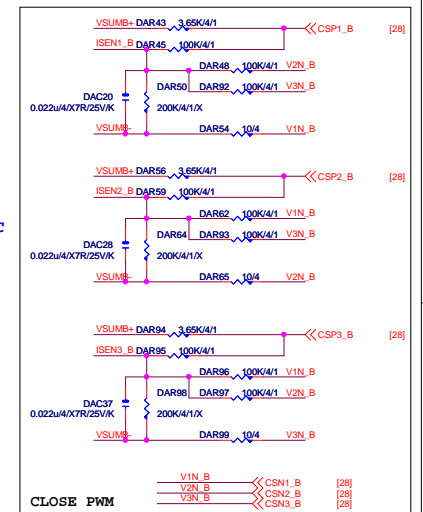
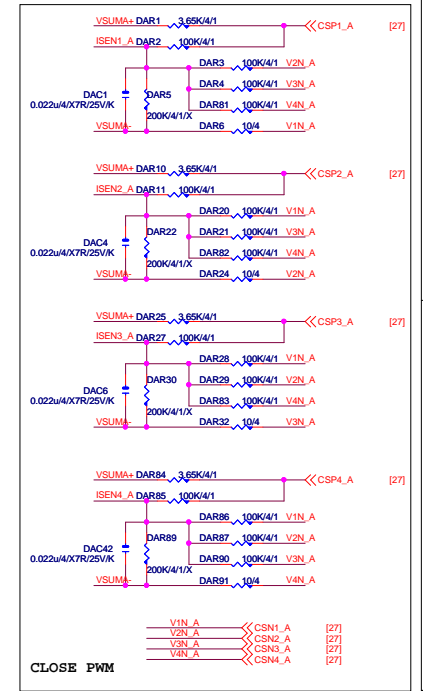
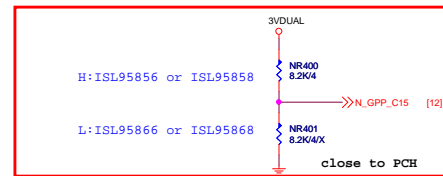
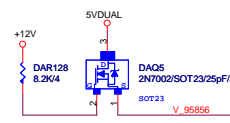
Footprint : HOLE\_C236D165-A



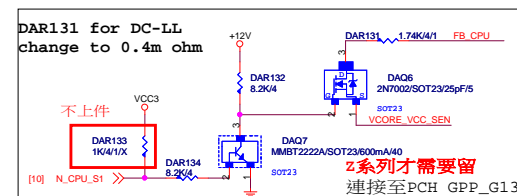
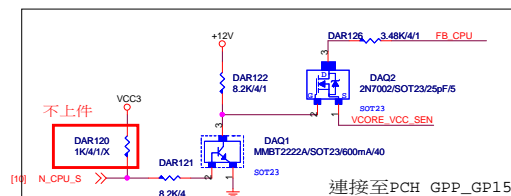
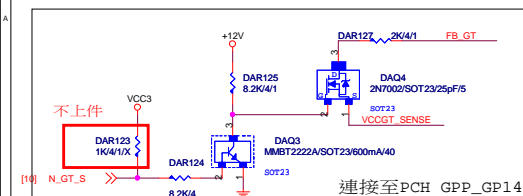
DIP螺絲



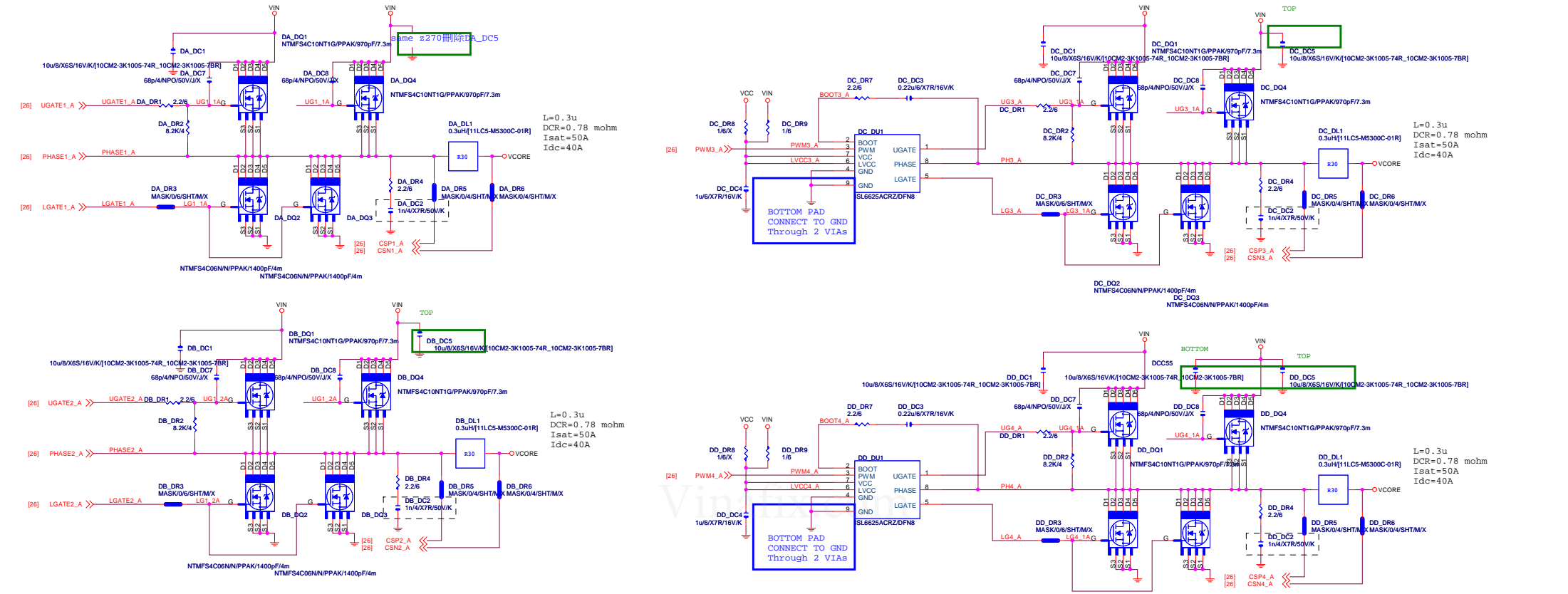
SATA 5 (文字面寫SATA 1)  
SATA 4 (文字面寫SATA 0)  
SATA 3  
SATA 2  
SATA 1 (文字面寫SATA 5)  
SATA 0 (文字面寫SATA 4)



VSCORE	ISL95856	ISL95866	VCCGT	ISL95856	ISL95866
DAR137	X	V	DAR140	X	V
DAR138	V	X	DAR141	V	X
DAR139	X	V	DAR142	X	V
DAC15	V	X	DAC27	V	X
DAR79	V	X	DAR80	V	X
DAR33	V	X	DAR51	V	X



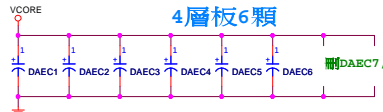
VCORE



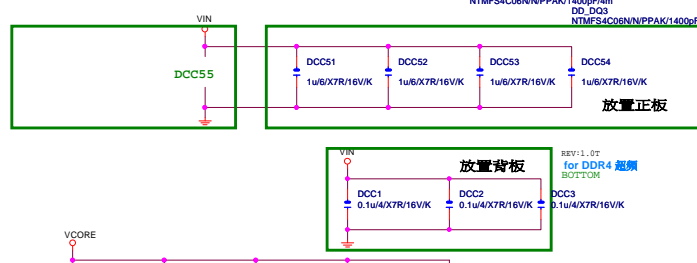
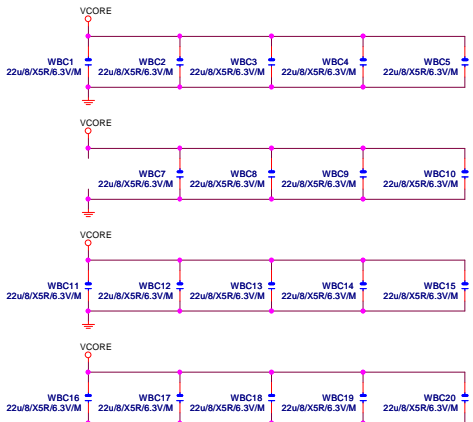
VCORE CAP

560u\*6PCS  
22u\*29PCS

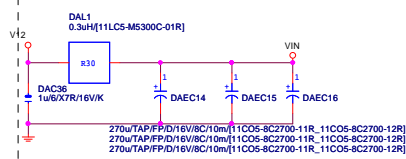
4層板6銅



560uTAP/PP/D/6.3V/697m[11CO2-695600-21R, 11CO2-695600-22R]  
560uTAP/PP/D/6.3V/697m[11CO2-695600-21R, 11CO2-695600-22R]  
560uTAP/PP/D/6.3V/697m[11CO2-695600-21R, 11CO2-695600-22R]  
560uTAP/PP/D/6.3V/697m[11CO2-695600-21R, 11CO2-695600-22R]  
560uTAP/PP/D/6.3V/697m[11CO2-695600-21R, 11CO2-695600-22R]  
560uTAP/PP/D/6.3V/697m[11CO2-695600-21R, 11CO2-695600-22R]



VIN CAP 270u\*3PCS



**GIGABYTE**

File: ISL95866\_MOS  
Size: Custom  
Document Number: Z370 HD3  
Date: Tuesday, August 01, 2017  
Sheet: 27 of 53

Diagram illustrating the circuit for a 100MHz 1T1G PPAK driver. The circuit includes a MOSFET driver IC (DN\_DU1, SL6625ACR2/DFN8) and two MOSFETs (DN\_DQ1, DN\_DQ2).

**Components and Connections:**

- Driver IC (DN\_DU1):**
  - Pin 2 (BOOT) connected to DN\_DR8 (16X) and DN\_DR9 (16).
  - Pin 3 (PWM) connected to PWM2\_B.
  - Pin 7 (VCC) connected to VCC.
  - Pin 6 (LVCC) connected to LVCC2\_B.
  - Pin 4 (GND) connected to GND.
  - Pin 9 (GND) connected to GND.
  - Pin 1 (UGATE) connected to DN\_DR1 (10u/8X/50V/JX) and DN\_DC1 (0.22u/6X/7R/16V/K).
  - Pin 8 (PHASE) connected to DN\_DR2 (8.2K/4).
  - Pin 5 (LGATE) connected to DN\_DR3 (10u/8X/50V/JX) and DN\_DC2 (0.22u/6X/7R/16V/K).
- MOSFETs (DN\_DQ1, DN\_DQ2):**
  - DN\_DQ1: NTFMFS4C10NT1G/PPAK/970pF/7.3m, 10u/8X/50V/JX, 0.22u/6X/7R/16V/K.
  - DN\_DQ2: NTFMFS4C06N/PPAK/1400pF/4m, 10u/8X/50V/JX, 0.22u/6X/7R/16V/K.
- Passive Components:**
  - Resistors: DN\_DR1 (10u/8X/50V/JX), DN\_DR2 (8.2K/4), DN\_DR3 (10u/8X/50V/JX), DN\_DR4 (2.26), DN\_DR5 (1n/4X/7R/50V/K), DN\_DR6 (1n/4X/7R/50V/K), DN\_DR7 (2.26), DN\_DR8 (16X), DN\_DR9 (16).
  - Capacitors: DN\_DC1 (0.22u/6X/7R/16V/K), DN\_DC2 (0.22u/6X/7R/16V/K), DN\_DC3 (0.22u/6X/7R/16V/K), DN\_DC4 (1u/6X/7R/16V/K), DN\_DC5 (0.22u/6X/7R/16V/K).
- Other Components:**
  - Resistor: R30 (0.3uH/11C/LS-M5300C-01R).
  - Capacitor: CSP2\_B (0.22u/6X/7R/16V/K).

**Notes:**

- Bottom pad connect to GND through 2 vias.
- Parameters:  $L = 0.3\mu$ ,  $DCR = 0.78$  mohm,  $I_{sat} = 50A$ ,  $I_{dc} = 40A$ .

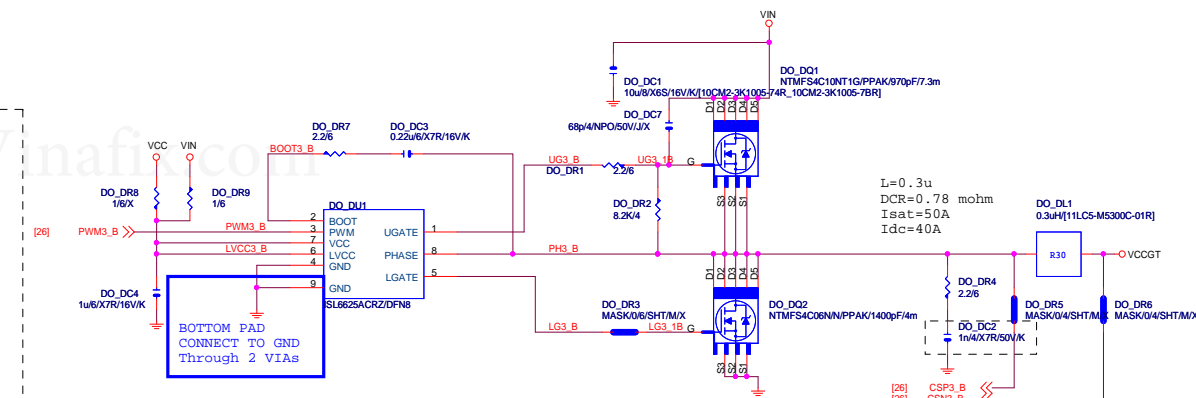
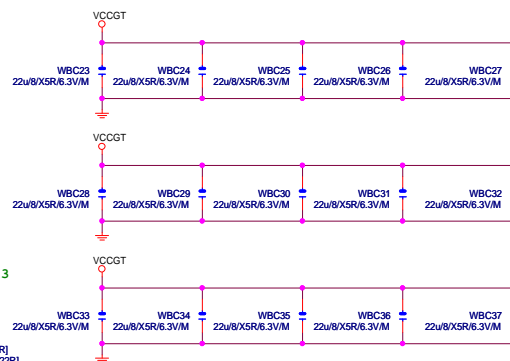
4層板3顆


VCCG

4層板3顆

DAEC9 DAEC10 DAEC11 DAEC12, DAEC13

560u7AP/FP/D6.3V/697m[11C02-695600-21R, 11C02-695600-22R]  
560u7AP/FP/D6.3V/697m[11C02-695600-21R, 11C02-695600-22]  
560u7AP/FP/D6.3V/697m[11C02-695600-21R, 11C02-695600-22]



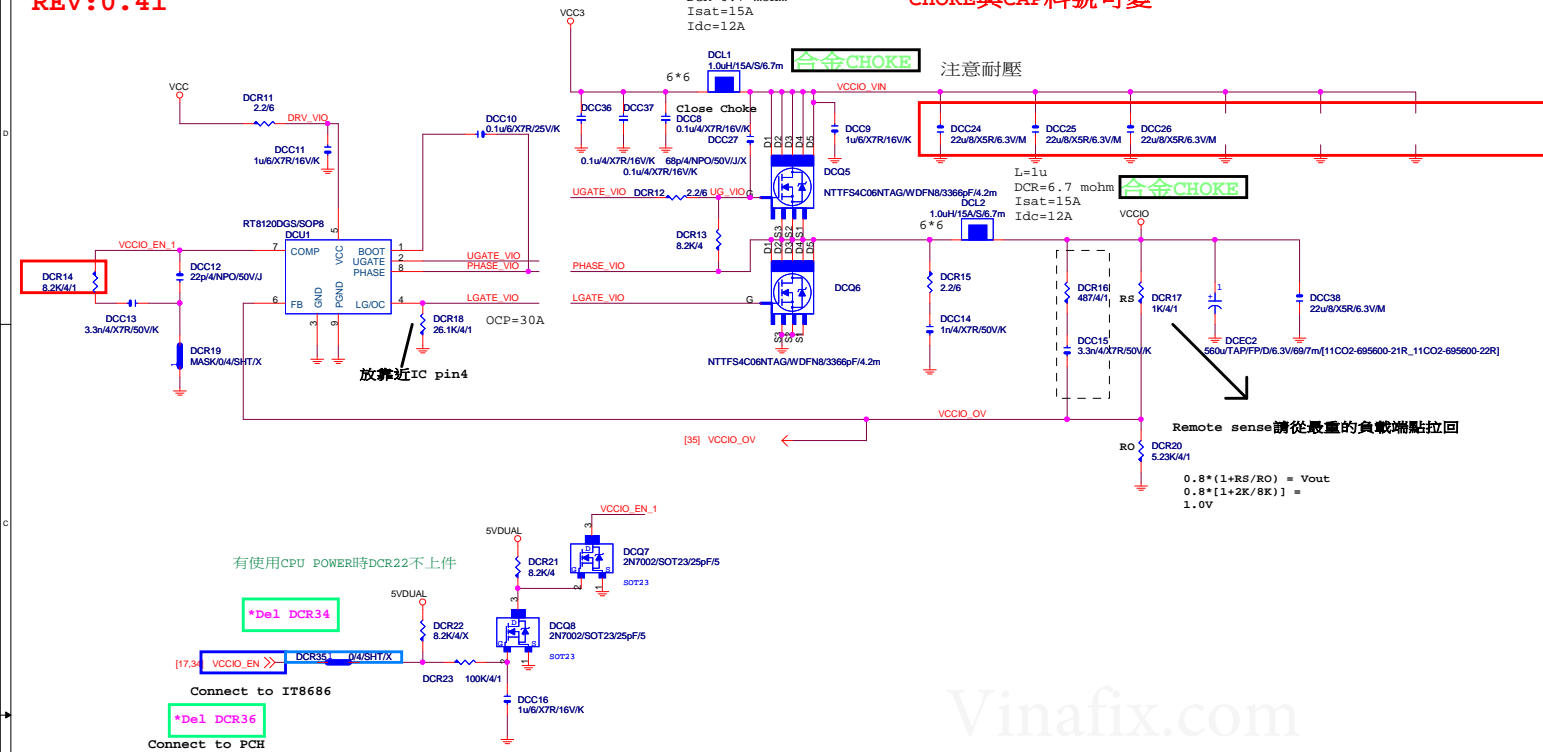
			
Title			
ISL95866_MOS			
Size	Document Number		Rev
Custom	Z370 HD3		1.0
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VCCIO

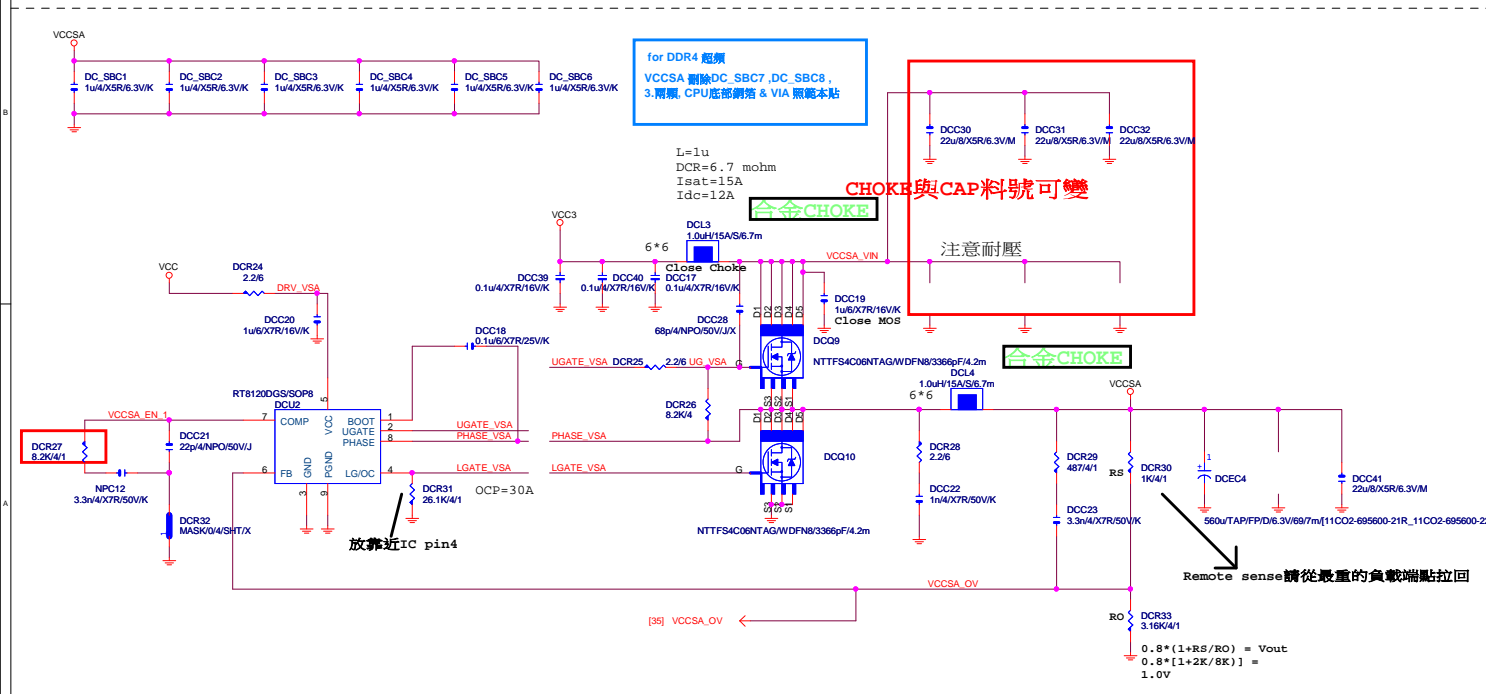
REV:0.41

L=1u  
DCR=6.7 mohm  
Isat=15A  
Idc=12A

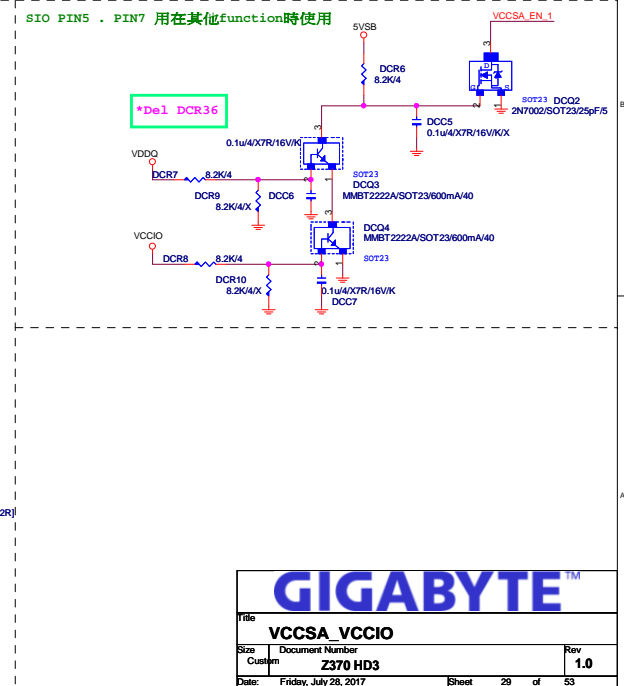
CHOKE與CAP料號可變



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SIO PIN5 . PIN7 用在其他function時使用



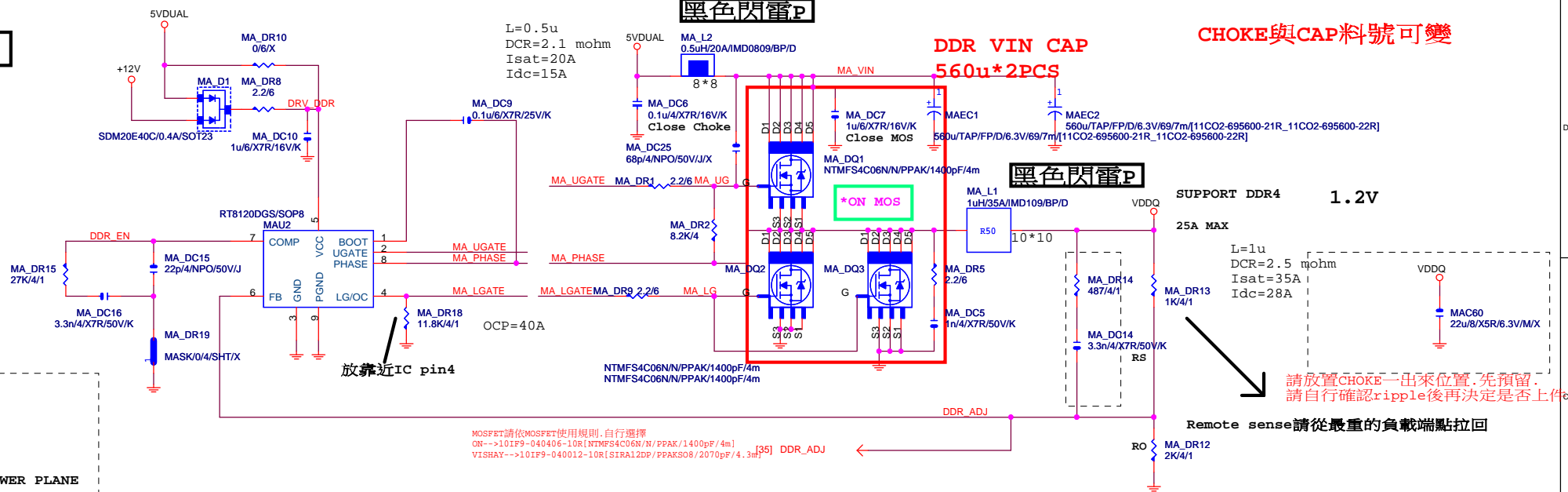
GIGABYTE™

File	VCCSA_VCCIO		Rev
Size	Document Number	Z370 HD3	
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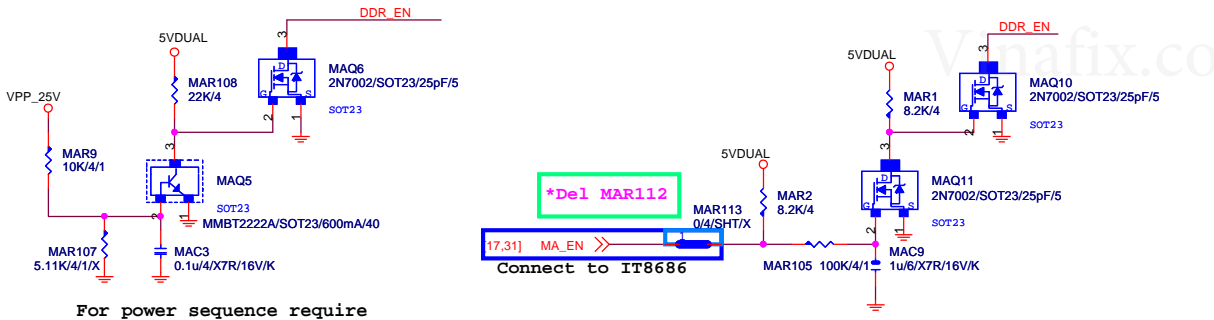


REV:0.4

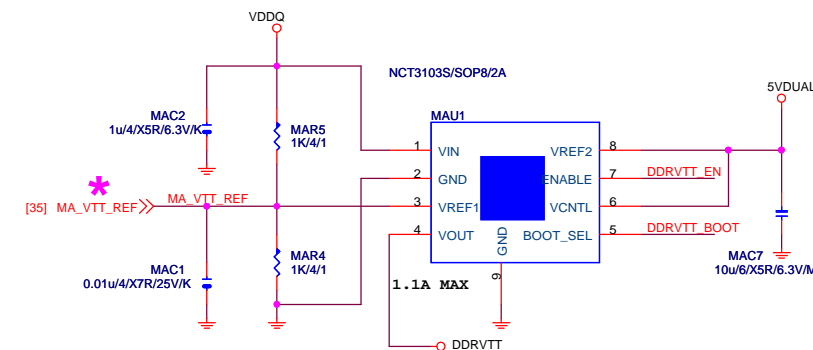
DDR4



PWR SEQ

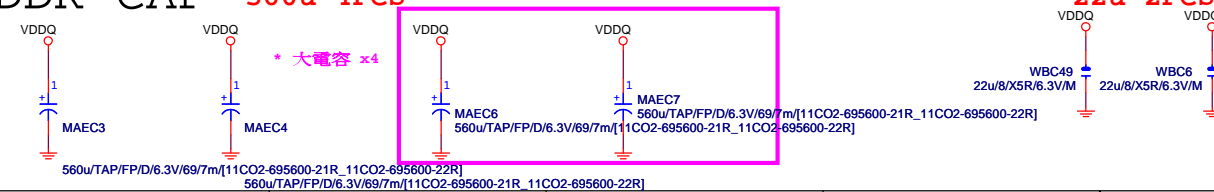


DDRVTT

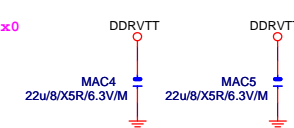


DDR CAP 560u\*4PCS

\*Footprint : EC6D8MM-RH-2



DDRVTT CAP



[4] DDR\_VTT\_CTL MAR110 0/4/SHT/M/X  
[7,51] N\_SLP\_S3 MAR111 DDRVTT EN  
MAU1上NCT3103S時上件

GIGABYTE™			
RT8120_DDR4 POWER			
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REV:0.4

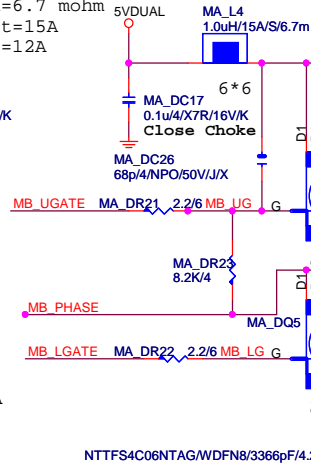
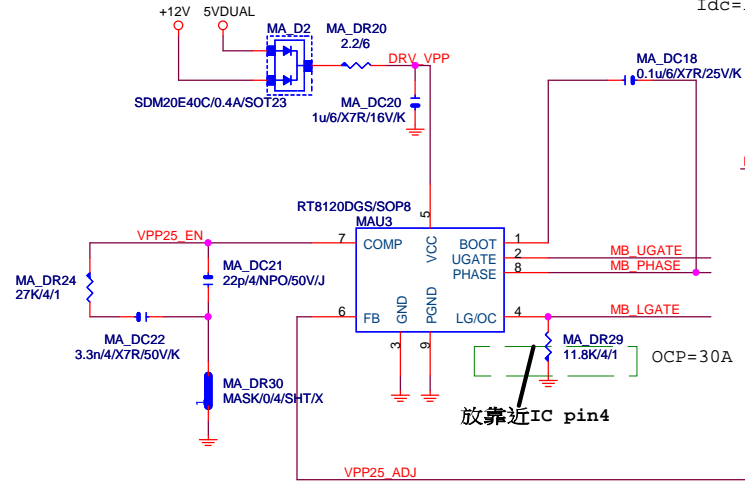
VPP\_25V

L=1u  
DCR=6.7 mohm  
Isat=15A  
Idc=12A

4. VPP\_25V CHOKe footprint 改CHOKe6X6mm\_SMD-1

合金CHOKe

CHOKe與CAP料號可變

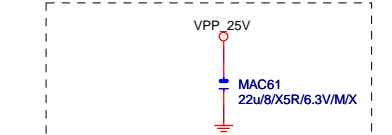
DDR\_VPP VIN CAP  
560u\*1PCS

L=1u  
DCR=6.7 mohm  
Isat=15A  
Idc=12A

$V_{(BR)DSS}$	$R_{DS(on) MAX}$	$I_D MAX$
30 V	4.2 mΩ @ 10 V	67 A
	6.1 mΩ @ 4.5 V	

SUPPORT DDR4 2.5V

VPP\_25V 25A MAX

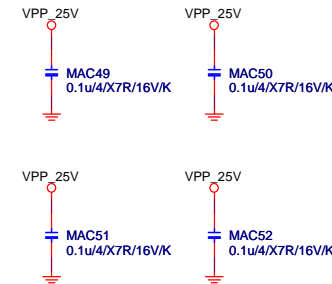
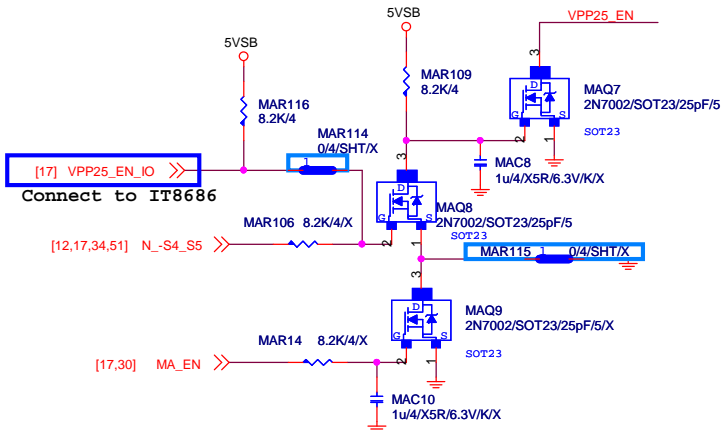


Remote sense請從最重的負載端點拉回

[35] VPP25\_ADJ ← VPP25\_ADJ

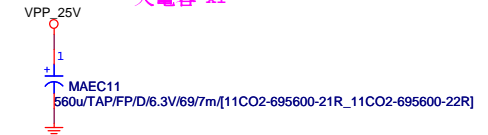
PWR SEQ

\* 刪 MA\_DR32



VPP CAP 560u\*1PCS

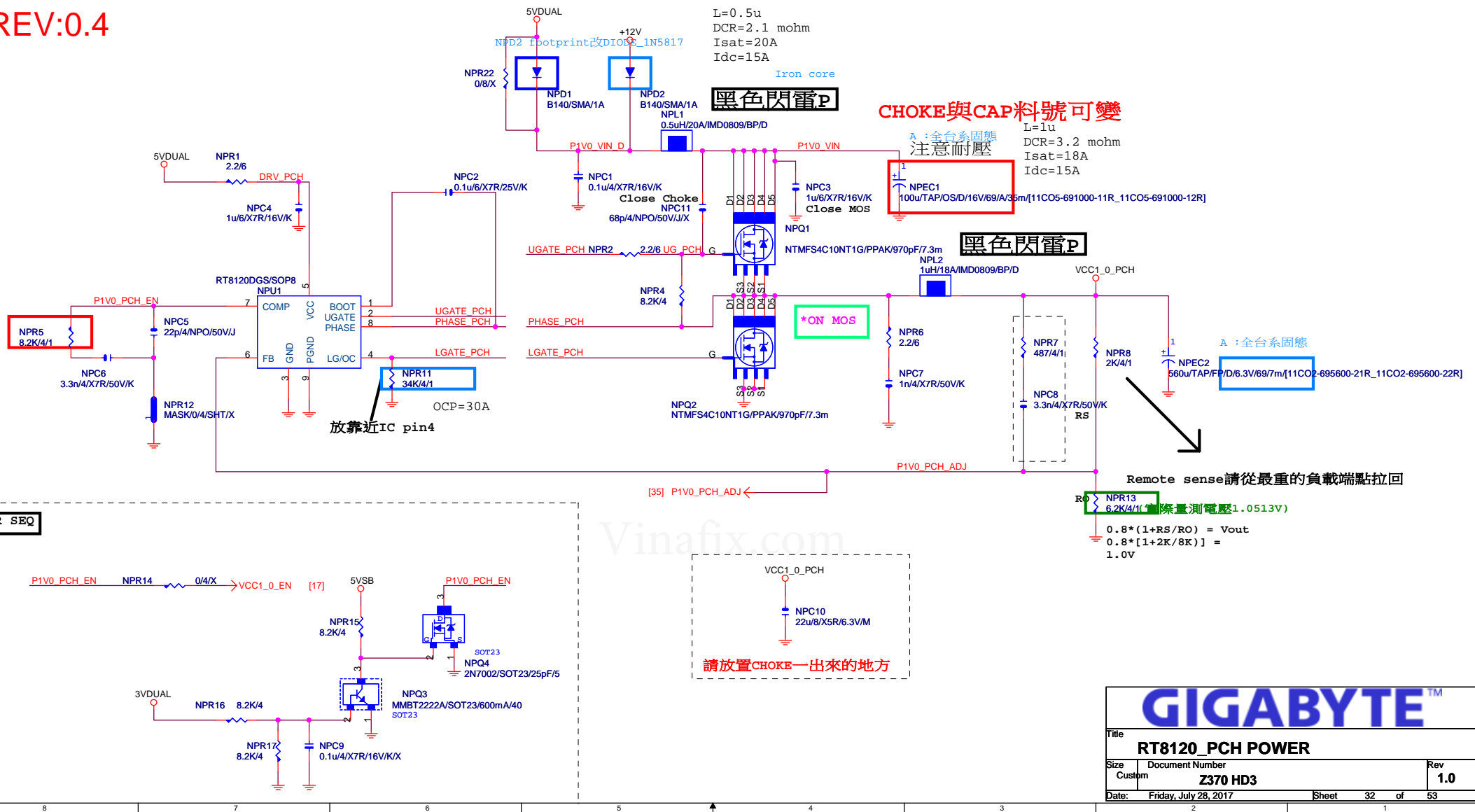
\* 大電容 x1

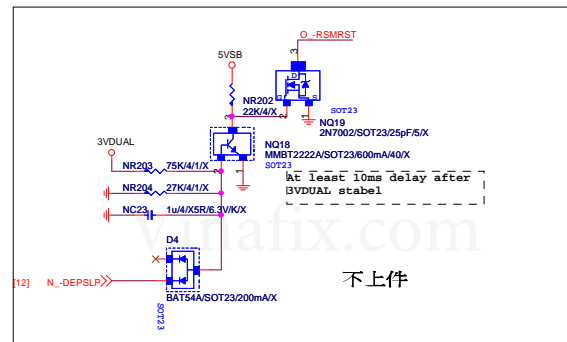
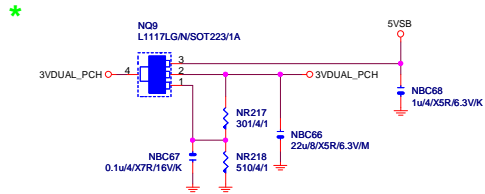
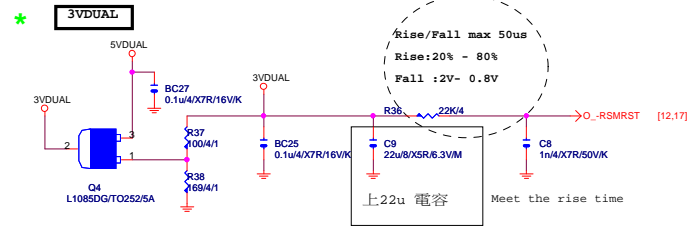
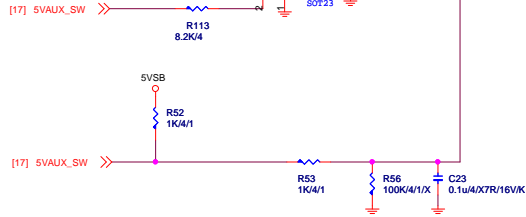


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Title	RT8120_VPP25 POWER	
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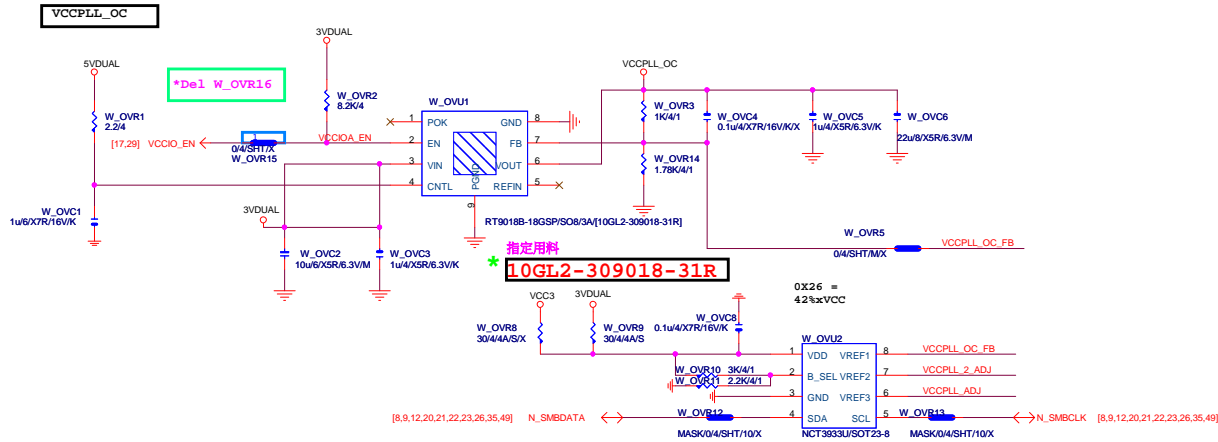
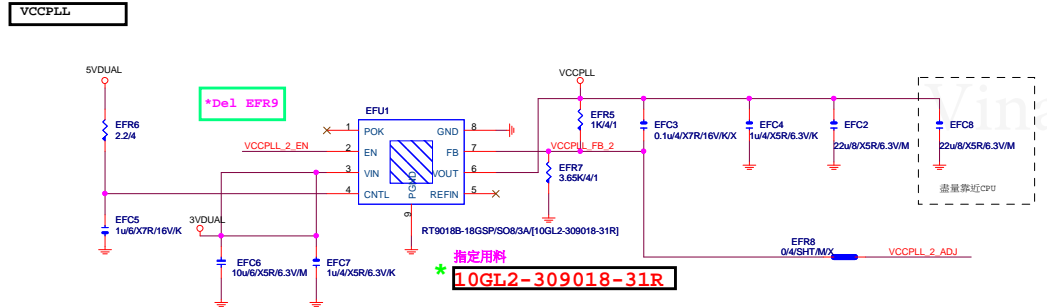
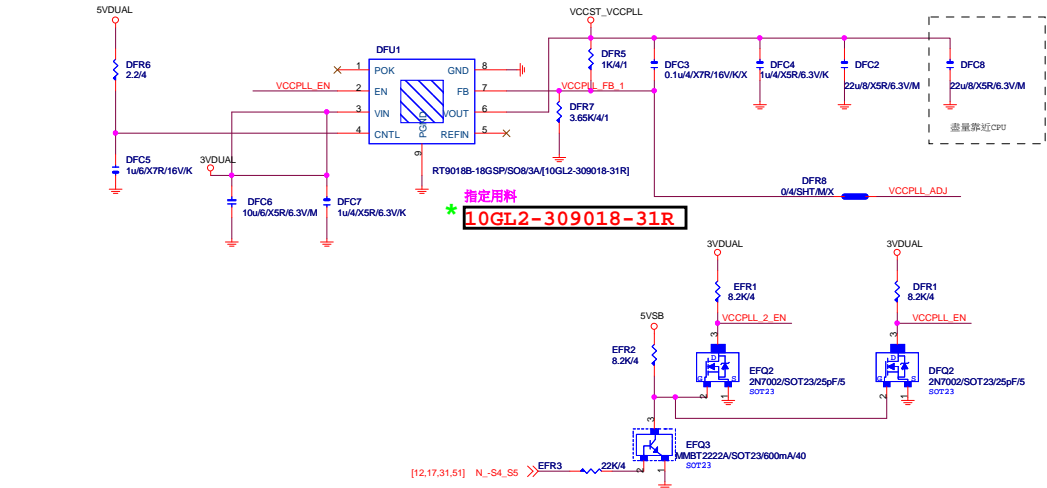
REV:0.4



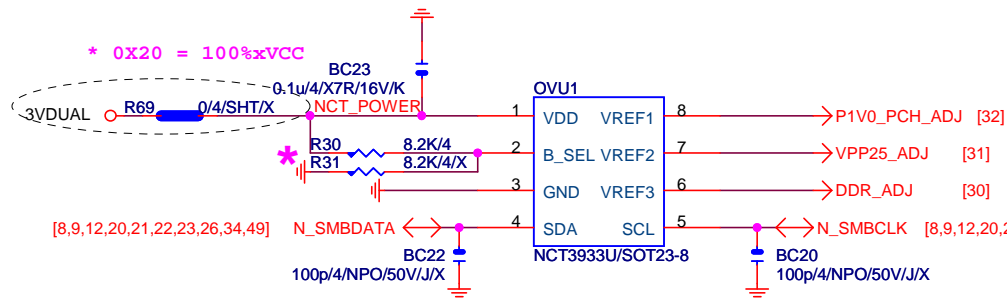


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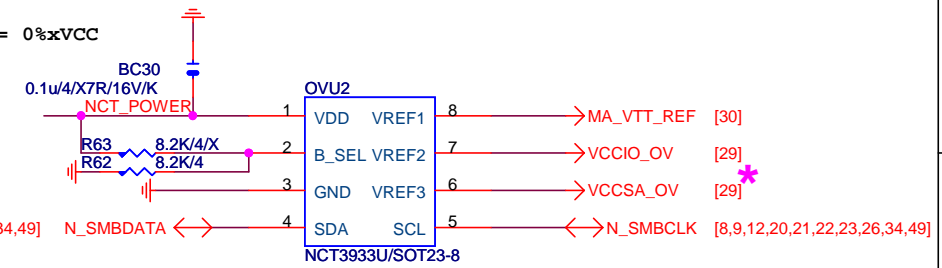
VCCST\_VCCPLL 替換原先MOS開關線路



# OVER VOLTAGE



0X2A = 0%xVCC



0X22 = 75%xVCC

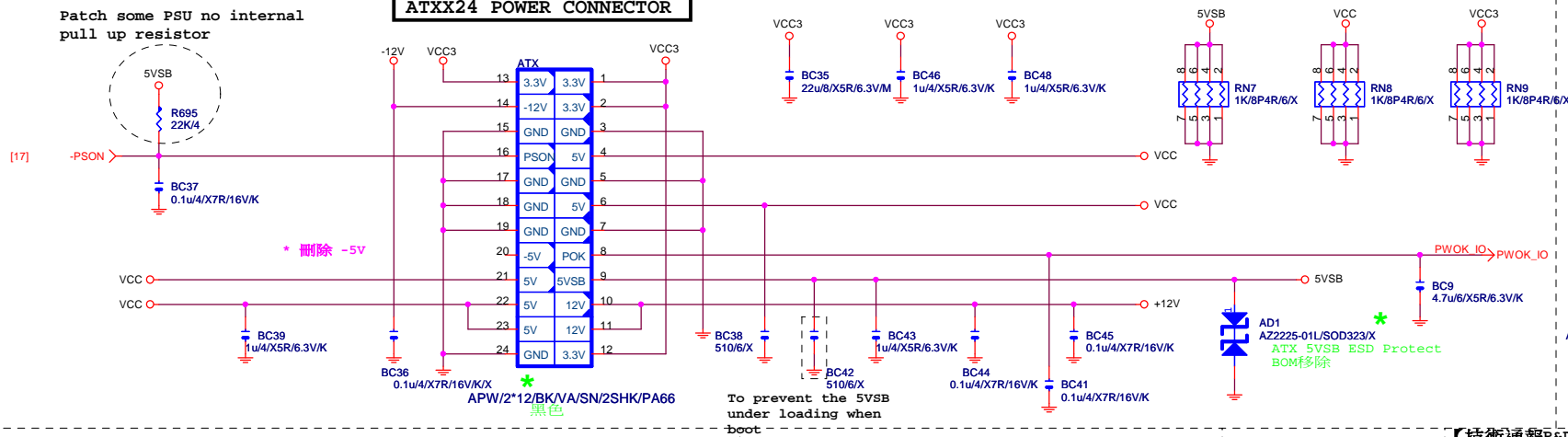
\* 删除 OVU3

NCT3933	0X20	0X2A
VREF1	VCC1_0_PCH	DDRVTT
VREF2	VPP_25V	VCCIO
VREF3	VDDQ	VCCSA

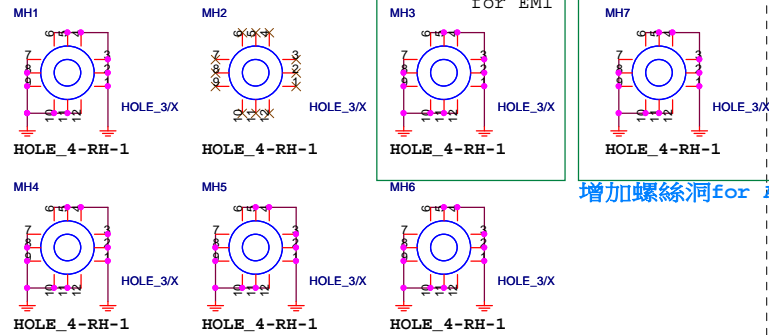
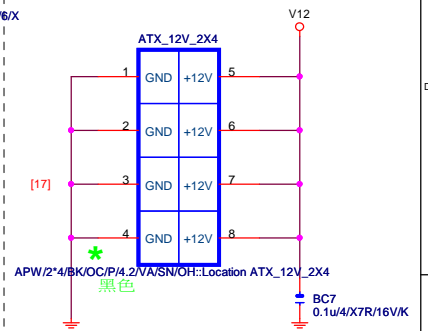
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Gigabyte Technology		
Title CPU CORE VR-2		
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# ATXX24 POWER CONNECTOR

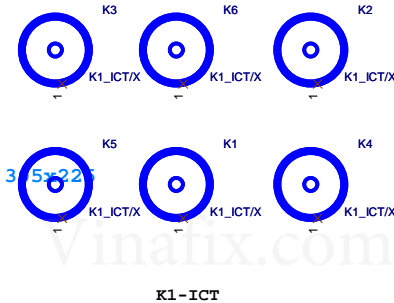


# ATXX4 POWER CONNECTOR



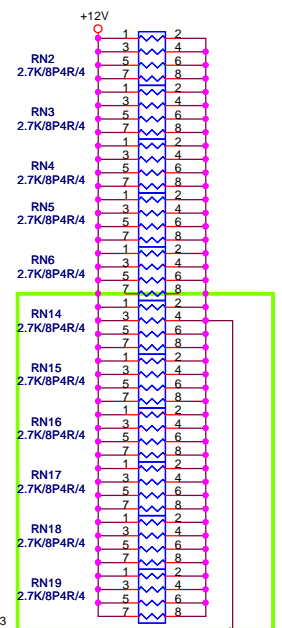
增加螺絲洞for ATX 3.5x22.5

有TYPE-C螺絲洞改半圈, footprint :HOLE\_4-RH-5MM-2



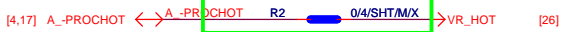
# 【技術通報R&D技術通報153】

To fix 12V light load abnormal issue

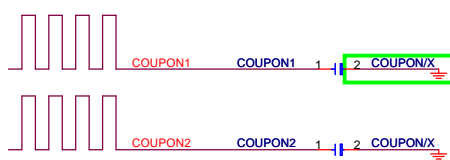


\* For China POWER

# -PROHOT



# COUPON



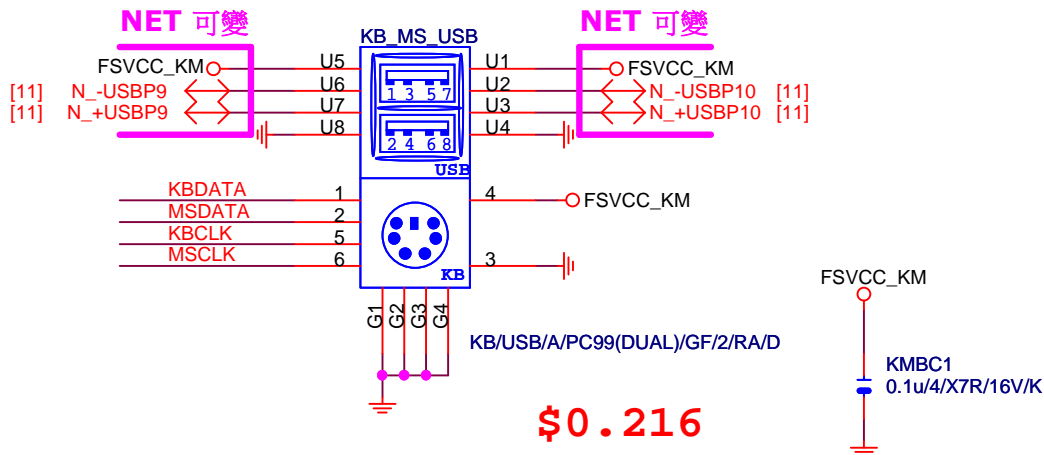
# Gigabyte Technology

Title		
ATX POWER CONNECTOR		
Size	Document Number	Rev
Custom	Z370 HD3	1.0
Date:	Friday, August 04, 2017	Sheet 36 of 53



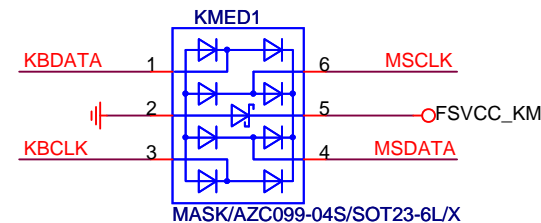
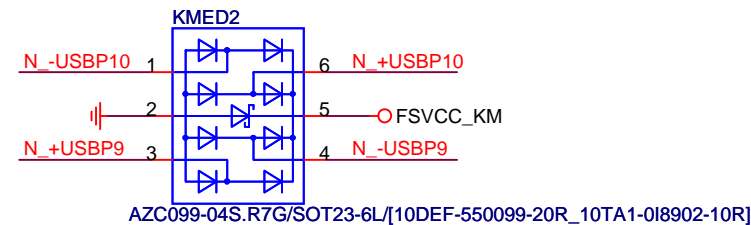
KB\_MS\_USB

Rev: 0.2

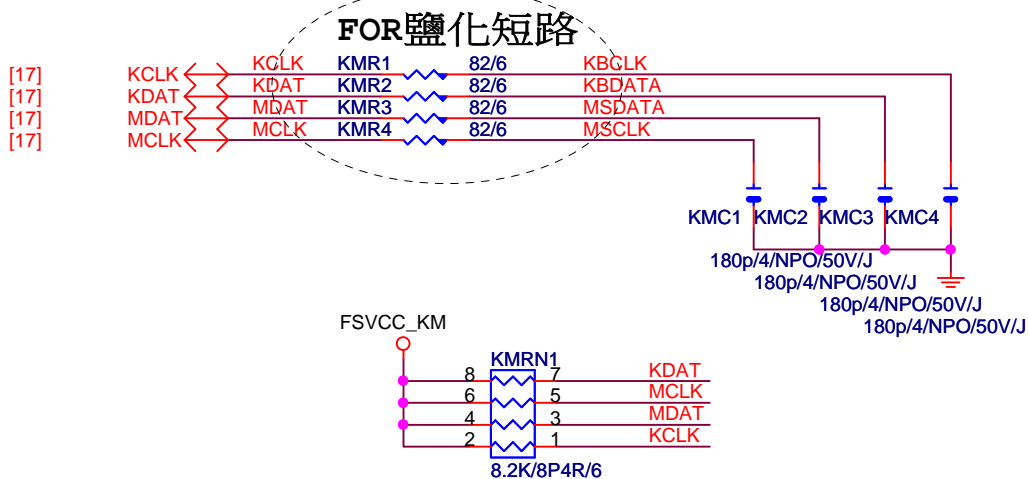


ESD

\*SWAP KMED2

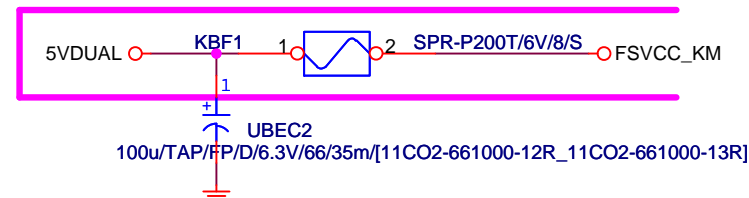


KB\_MS\_USB DAMPING/PU

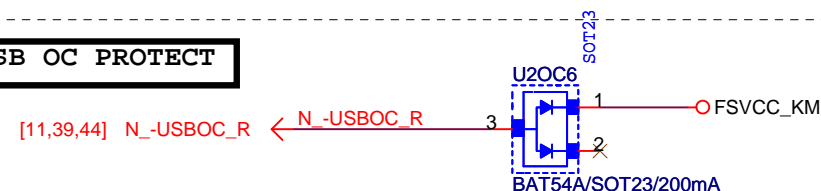


KB\_MS\_USB PWR

NET 可變, 與其他USB SHARE



USB OC PROTECT



Gigabyte Technology

Title

AUDIO JACK

Size  
A

Document Number

Z370 HD3

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1.0

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Impedance=85  $\pm$  17.5%

Port	Port Label	Port Type	Port Description	Port Speed	Port Status	Port Color	Port Label	Port Type	Port Description	Port Speed	Port Status	Port Color
[4]	DVI_TXC	YBC1	0.1u4/X7R/16V/K	DVITXC+	VR1	680/4/1						
[4]	DVI_TXC	YBC2	0.1u4/X7R/16V/K	DVITXC-	VR2	680/4/1						
[4]	DVI_TX0	YBC3	0.1u4/X7R/16V/K	DVITX0+	VR3	680/4/1						
[4]	DVI_TX0	YBC4	0.1u4/X7R/16V/K	DVITX0-	VR4	680/4/1						
[4]	DVI_TX1	YBC5	0.1u4/X7R/16V/K	DVITX1+	VR7	680/4/1						
[4]	DVI_TX1	YBC7	0.1u4/X7R/16V/K	DVITX1-	VR8	680/4/1						
[4]	DVI_TX2	YBC8	0.1u4/X7R/16V/K	DVITX2+	VR9	680/4/1						
[4]	DVI_TX2	YBC9	0.1u4/X7R/16V/K	DVITX2-	VR10	680/4/1						

VBC6  
0.1u/4/X7R/16V/K/X

The schematic shows a horizontal magenta line representing the FSVCC\_KM power rail. A red wire connects this rail to a capacitor symbol labeled VBC10. Below the capacitor, the text '0.1u/X7R/16V/K' specifies the capacitor's value, dielectric material, voltage rating, and tolerance. The other terminal of the capacitor is connected to a ground symbol.

Pin configuration diagram for the VESD3 component. The component has 6 pins. Pin 1 is connected to DVI\_HP. Pin 2 is connected to DVI\_SCL. Pin 3 is connected to DVI\_HP. Pin 4 is connected to DVI\_SDA. Pin 5 is connected to FSVCC\_KM. Pin 6 is connected to DVI\_SCL. A dashed oval encloses pins 4, 5, and 6, labeled "NET 可變".

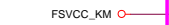
ACZ099-04S.R7G/SOT23-6L[10DEF-550099-20R\_10TA1-0!8902-10R]

AZC099-04S.R7G/SOT23-6L[10DEF-550099-20R\_10TA1-0I8902-10R]

★Update 2016.06.20

★Update 2016.06.20

VCC VR19 8.2K/4 VQ4\_2 1 N\_DVI\_HDP\_F N\_DVI\_HDP\_F [10]



Footprint : DVI-30P-4P-1

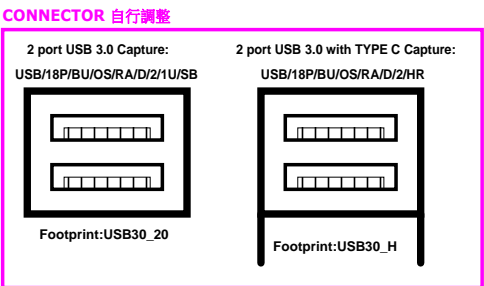
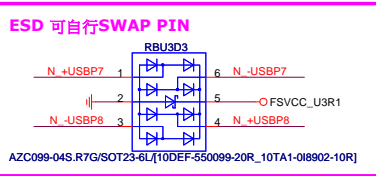
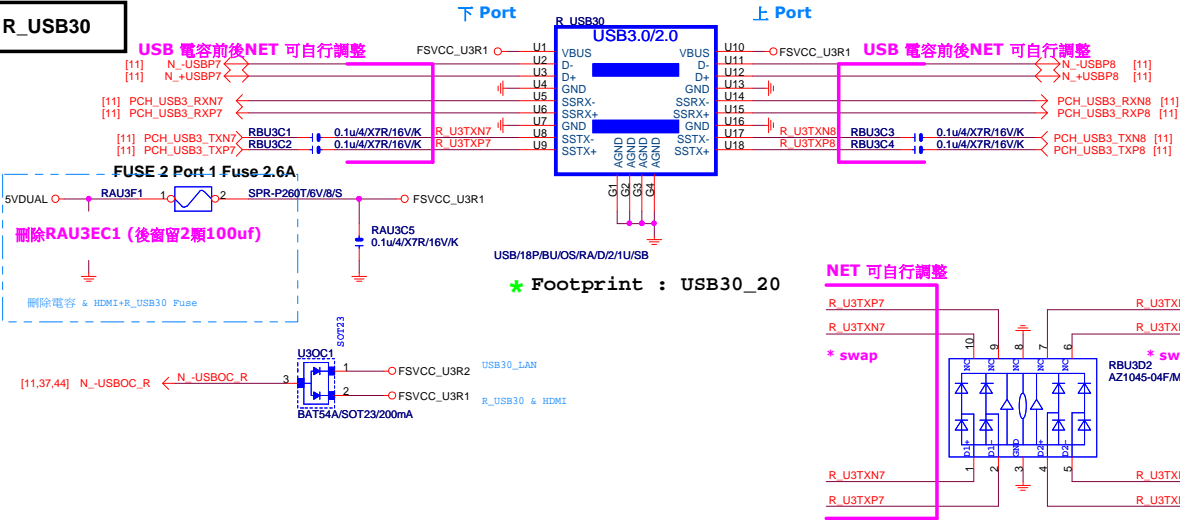
### 平躺式 DVI-D

11NR6-501024-31

## Gigabyte Technology

Title			
DVI			
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Date:	Friday, July 28, 2017	Sheet	38 of 53

R\_USB30



R\_USB30\_2

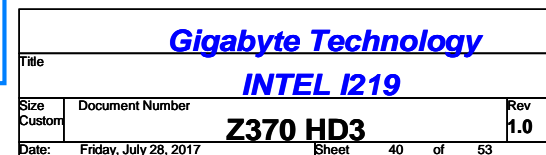
KB\_MS\_USB3

Vinafix.com

LAREQ1



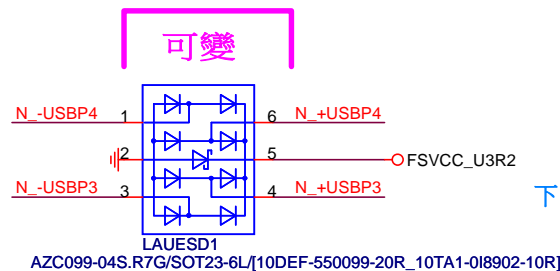
\*Add 25KV ESD



## R2.01

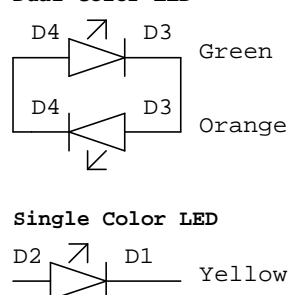
note:可變更USB NAME

note:可變更USB NAME



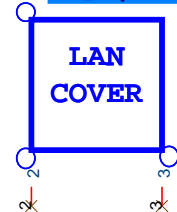
USB上白下藍:USB3+LAN/1G/GO,Y/OS/RA/D/G30/15KV/Q FLASH

## Dual Color LED



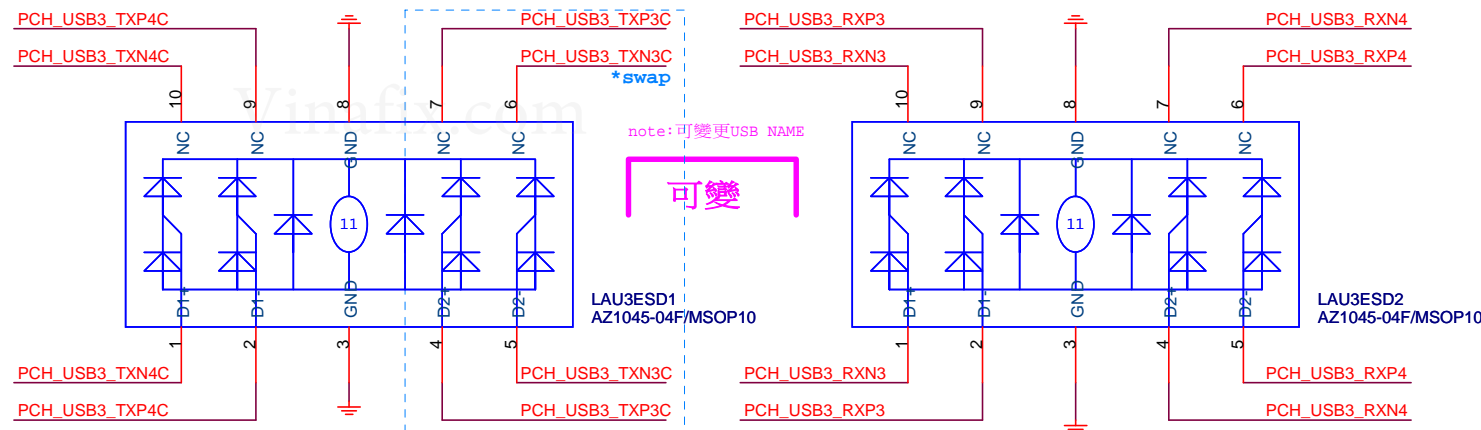
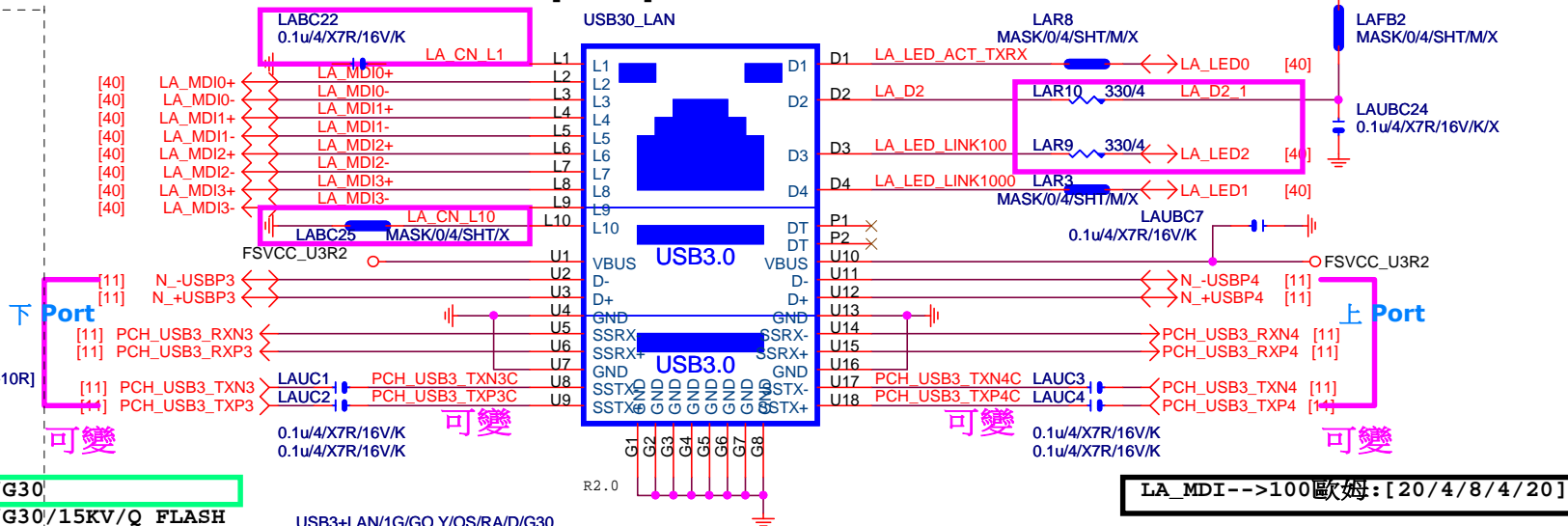
FOOT PRINT:LAN COVER

1 USB\_LAN\_HS  
LAN\_HS/[11NH1-LNC001-11R]/X

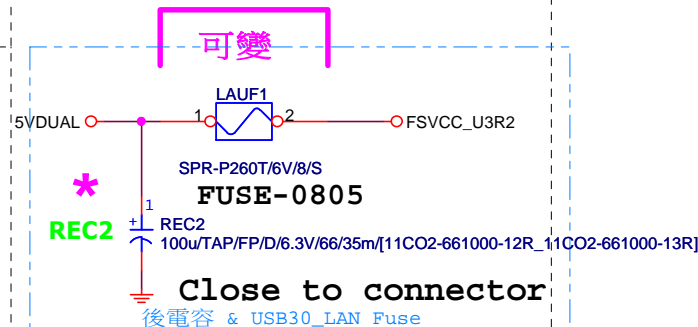


## 可變 [視SPEC需求]

## USB30\_LAN



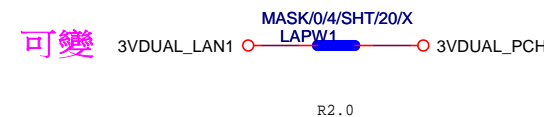
note:可變更FUSE



## LAN POWER

note: lan power連接及電流

For PVT :LAPW1 改 R0402-2-SHORT20



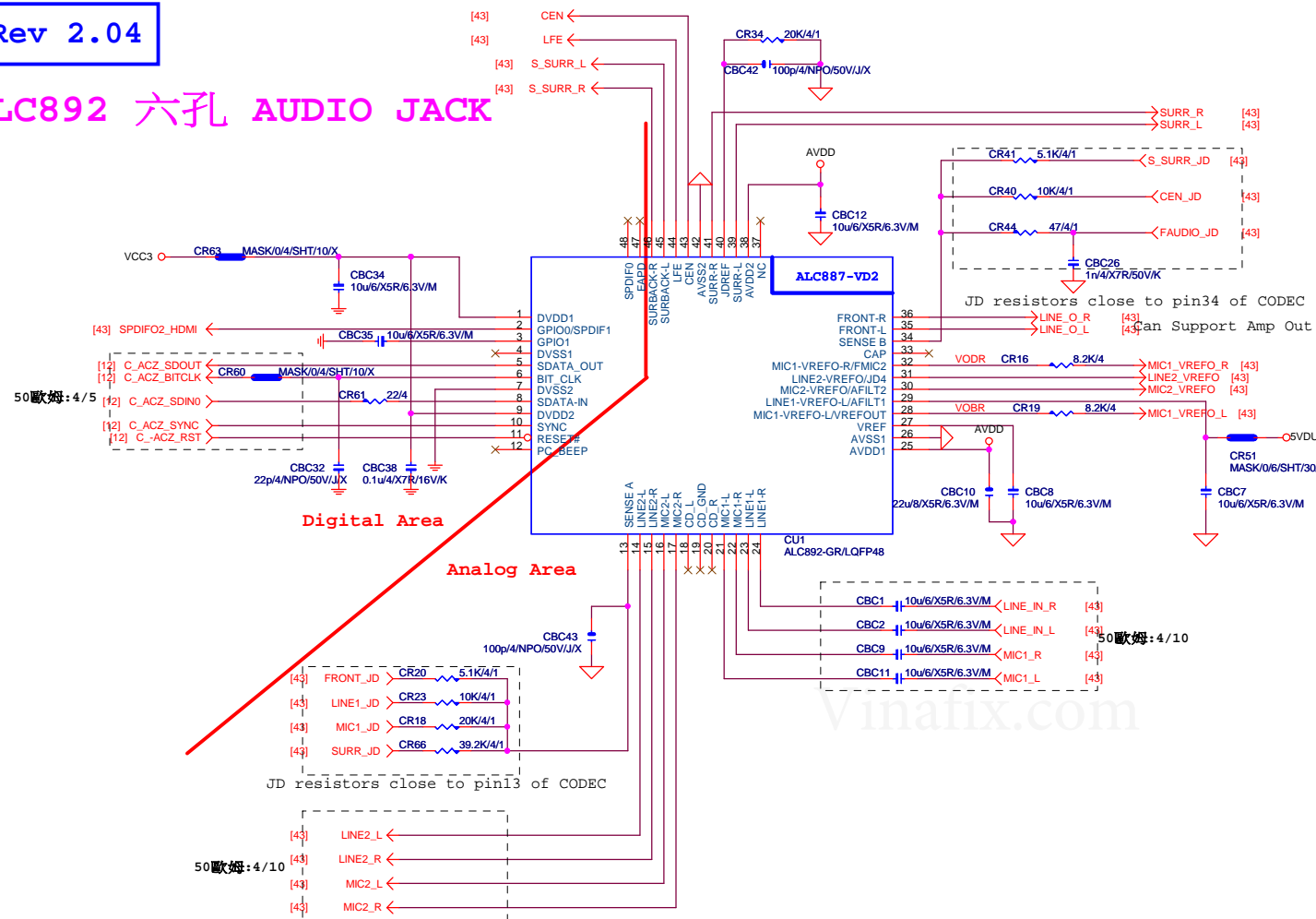
## Gigabyte Technology

## LAN CONNECTOR-INTEL I219

# Z370 HD3

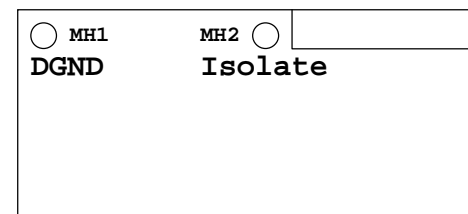
Size Custom	Document Number <b>Z370 HD3</b>	Rev 1.0
Date: Friday, July 28, 2017	Sheet 41 of 53	

## ALC892 六孔 AUDIO JACK



LAYOUT注意: 螺絲孔下GND方式

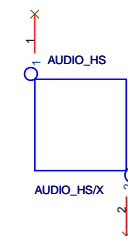
1. MH1空間夠, 下DGND  
空間不夠, 才改為Isolate
2. MH2一律改為Isolate
3. Codec下方, 第二層必須參考GND



LAYOUT注意: 要加

GND切割線

音效區域印刷

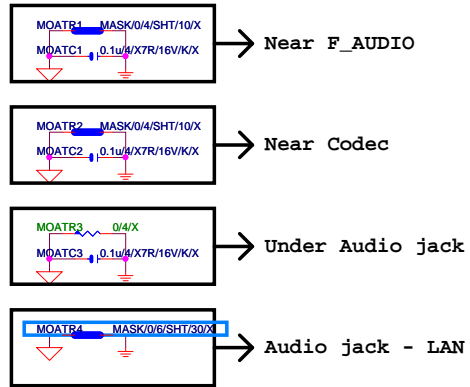


\*料號後補

www.teknisi-indonesia.com

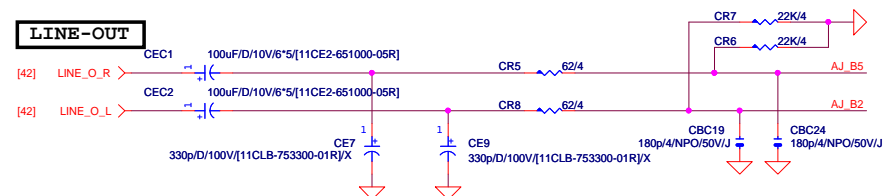
- BOM OPTION :
1. Chemicon音效電容
  2. 金屬外罩 Reserve (LAYOUT上件與否, 依照各Model spec)
  3. LED Reserve (上件與否和LED顏色, 依照各Model spec)

Gigabyte Technology			
Title HD AUDIO ALC892			
Size Custom	Document Number	Z370 HD3	
Date:	Friday, July 28, 2017	Sheet	42 of 53
		Rev	1.0



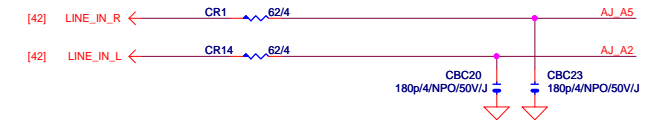
\*量産前,0ohm改short pad

## LINE-OUT

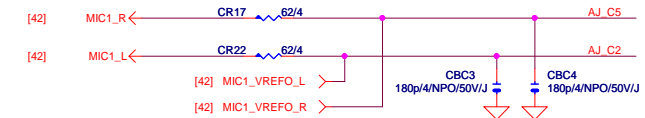


## LINE-IN

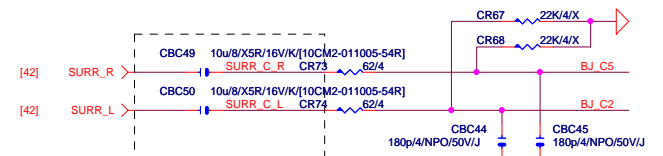
WIMA FOOTPRINT C2700PF-DIP-MASK



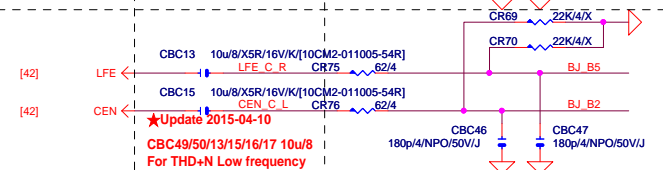
## MIC-IN



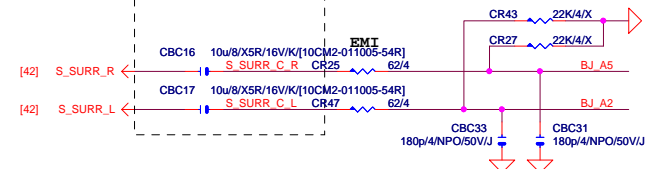
## SURROUND



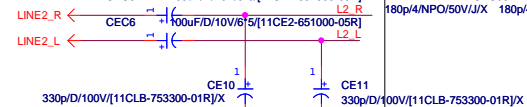
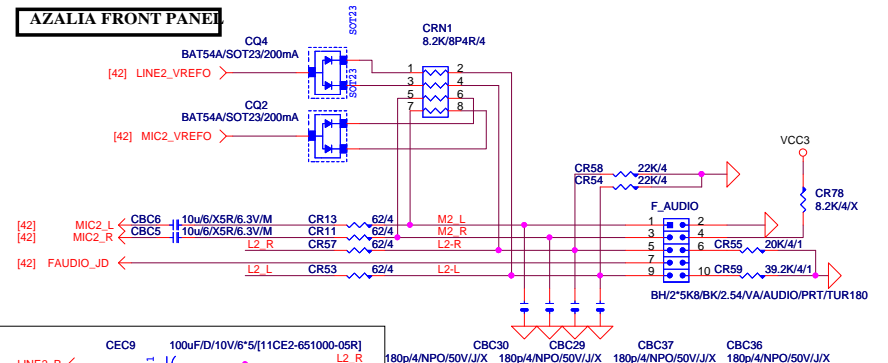
## CEN/LFE



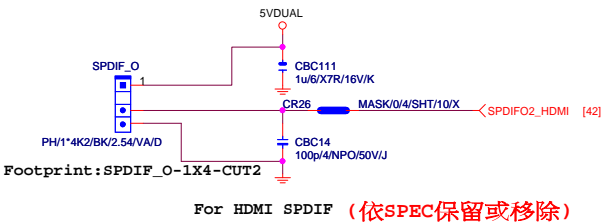
## SURR BACK



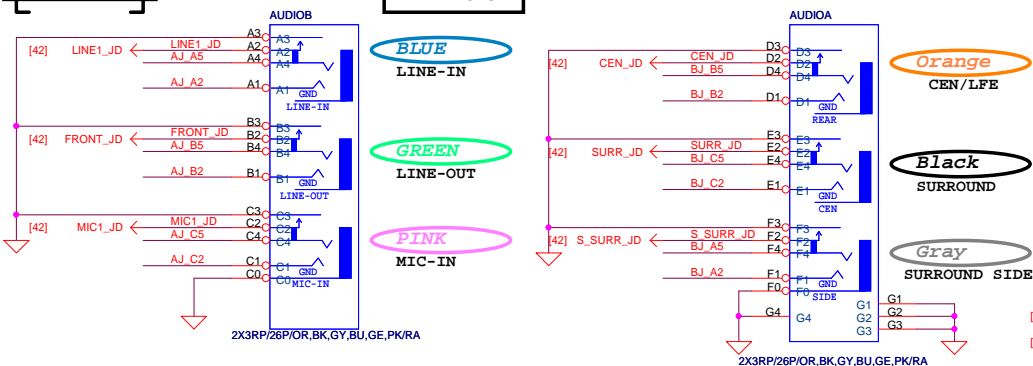
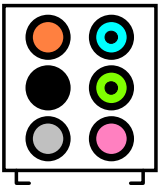
## AZALIA FRONT PANEL



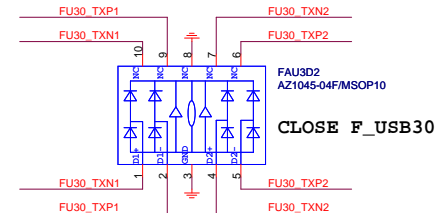
WIMA FOOTPRINT C2700PF-DIP-MASK



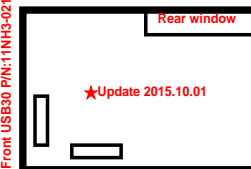
## AZALIA JACK



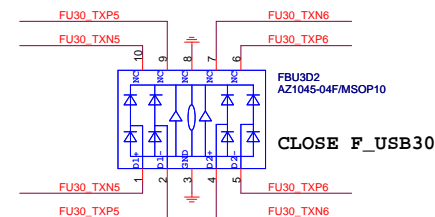




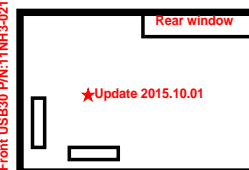
Front USB30 P/N:11NH3-021210-B1R/B2R



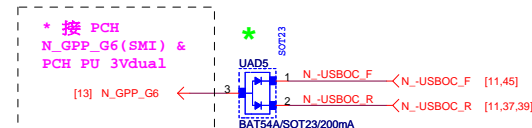
Front USB30 P/N:11NH3-021210-51R/52R



Front USB30 P/N:11NH3-021210-B1R/B2R

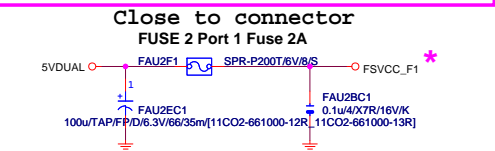
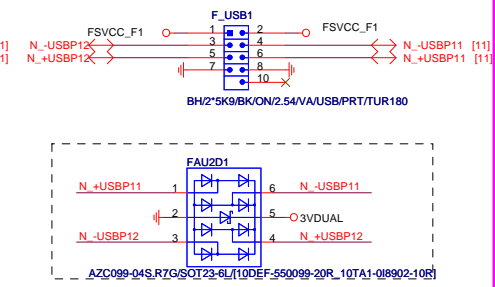


Front USB30 P/N:11NH3-021210-51R/52R



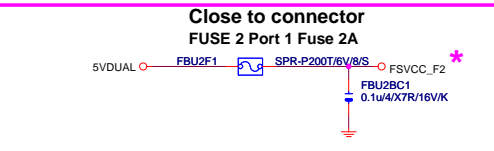
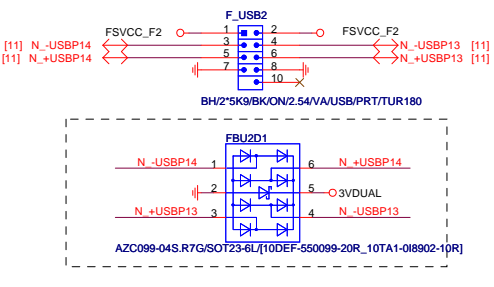
FRONT USB1

NET 可變



FRONT USB2

NET 可變



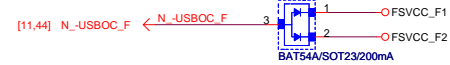
FRONT USB3

FRONT USB4

REAR USB1

REAR USB2

F\_USB 2.0 OC SIGNAL



Vinafix.com

## Rev: 0.2



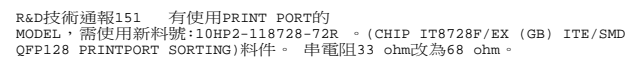
## COMA



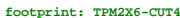
## N/A



## LPT PORT



## TPM CONNECT



## Thunderbolt

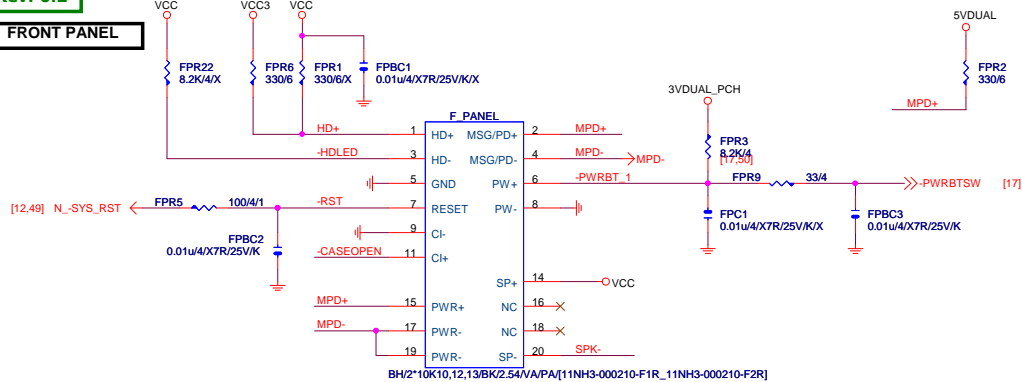
★Update 2015-12-29

```
* Del THB_C
```

Rev: 0.2

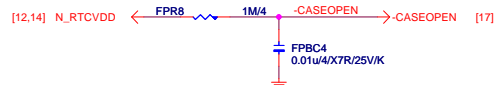
★Update 2016.06.15

## FRONT PANEL



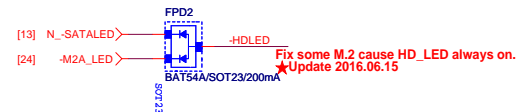
Update 2015.01.08  
Footprint=F\_PANEL-100

## CASE OPEN



## FRONT PANEL SHORT

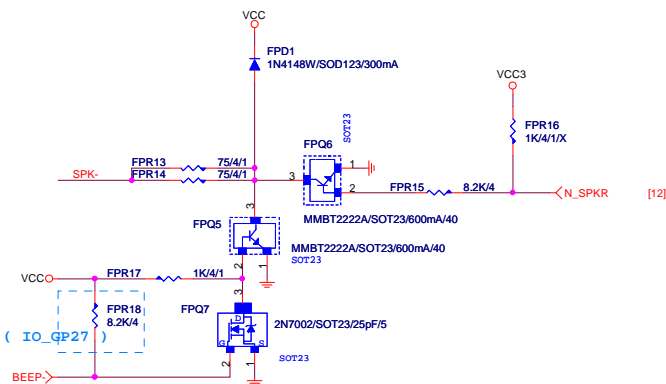
## SATA LED



Fix some M.2 cause HD\_LED always on.  
★Update 2016.06.15

## SPEAKER

For SPKR voltage issue. FPQ6=>2222, FPQ7=>7002

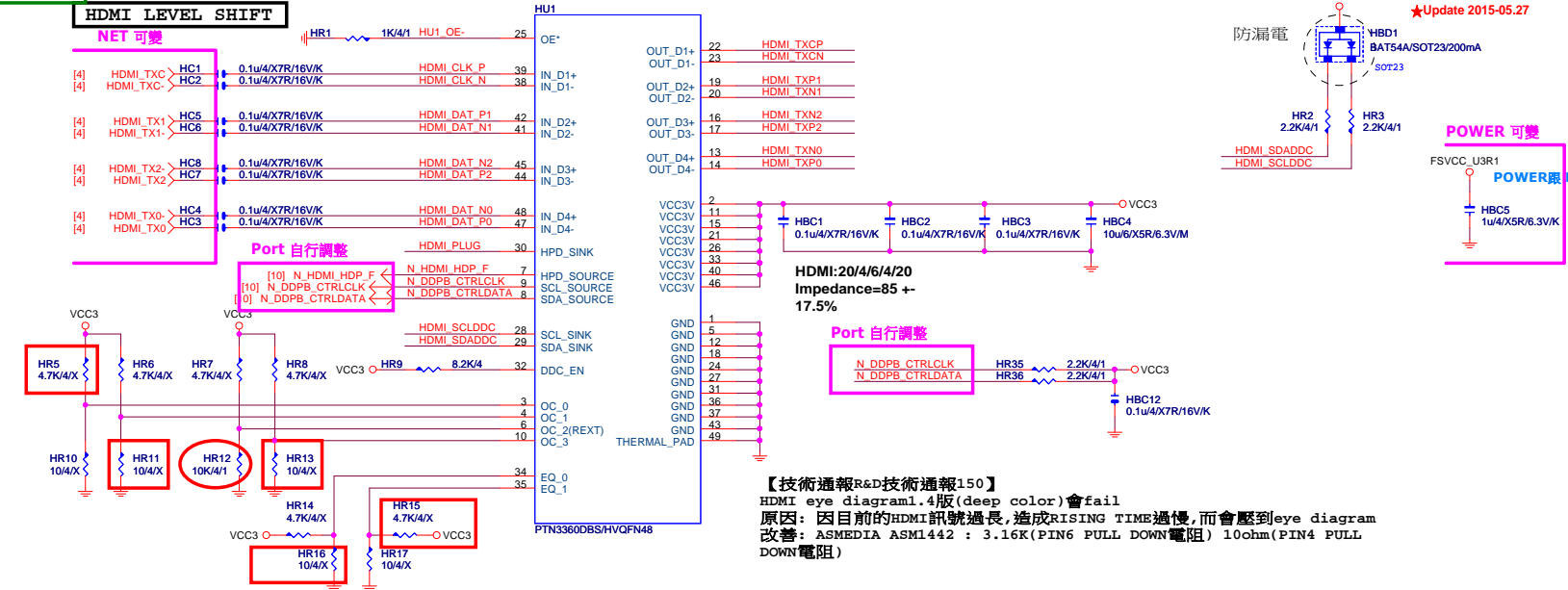


New , inport , Pull High ( IO\_GP27 )  
,IO\_GP26 ouport

For SPKR voltage issue. FPQ6=>2222, FPQ7=>7002

Gigabyte Technology

Title			
FRONT PANEL			
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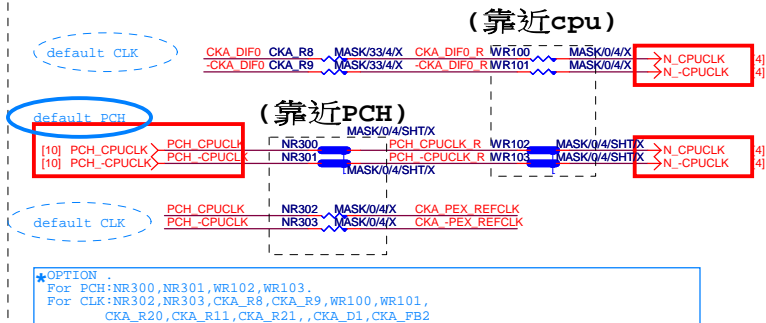
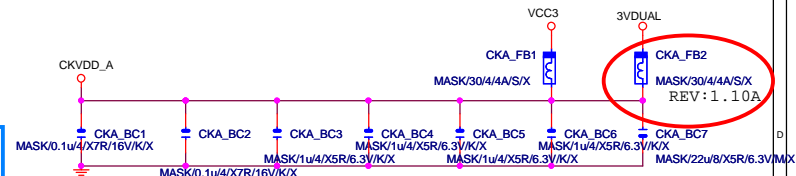
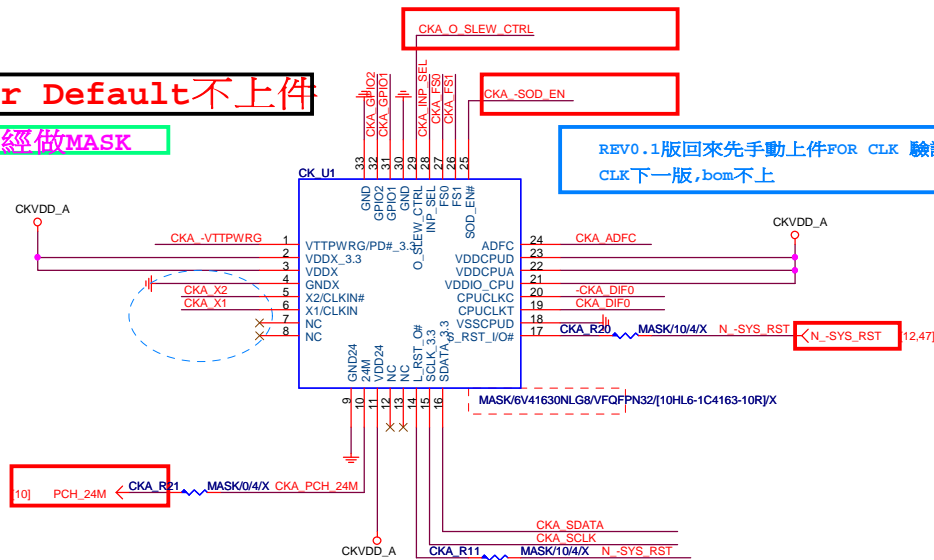
PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K  
ASM1442:紅色框要上,HR12:3.16K

Vinafix.com

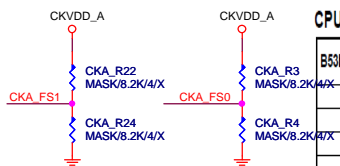
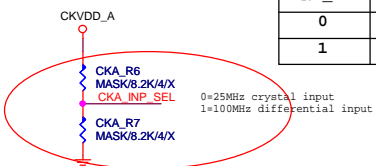
IDT6V41630

**\*CLK Buffer Default不上件**

不上件部分已經做MASK

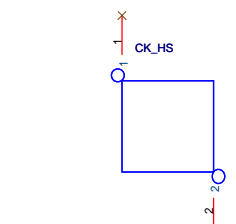
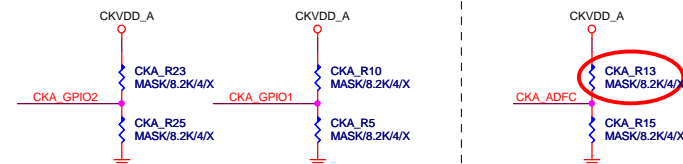


INP_SEL	Input
0	Crystal
1	CLK_INP/N

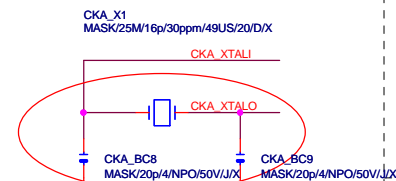


### CPU Frequency Selection and output Divider Table

B53b1(FS1)	B53b0(FS0)	VCO (MHz)	CPU Divider	CPU (MHz)	Typ SS%	Typ SS ON/OFF
0	0	200.00	2.00	100.00	-	OFF
0	1	400.00	4.00	100.00	-	OFF
1	0	1000.00	10.00	100.00	-5.00%	ON
1	1	100.00	1.00	100.00	-	OFF



\* CK\_HS/[11NH1-CBC001-01R]/X  
Footprint : CLOCK BUFFER COVER

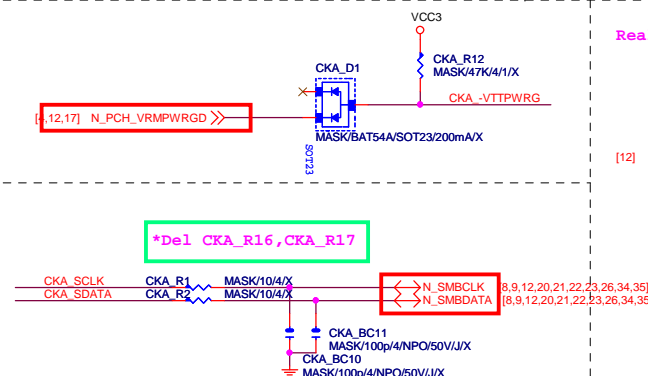


Defaults  
CKX1.CKBC8.CKBC9.CKR18.CKR19上件  
CKR30.CKR31不上件

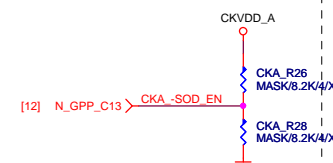


\*可變，依需求上件不上件。

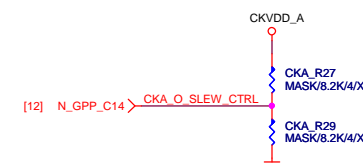
## SMBUS



### Real time selection function

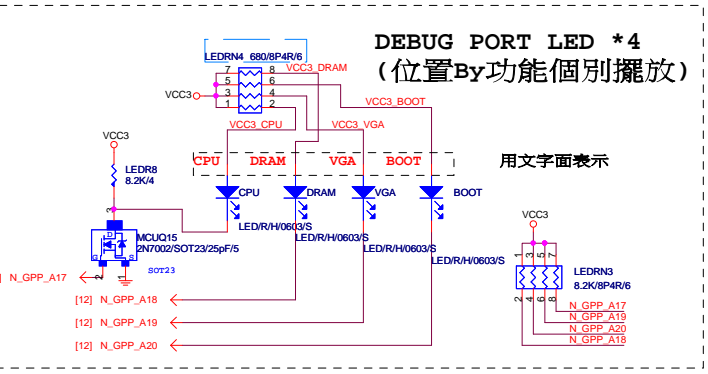
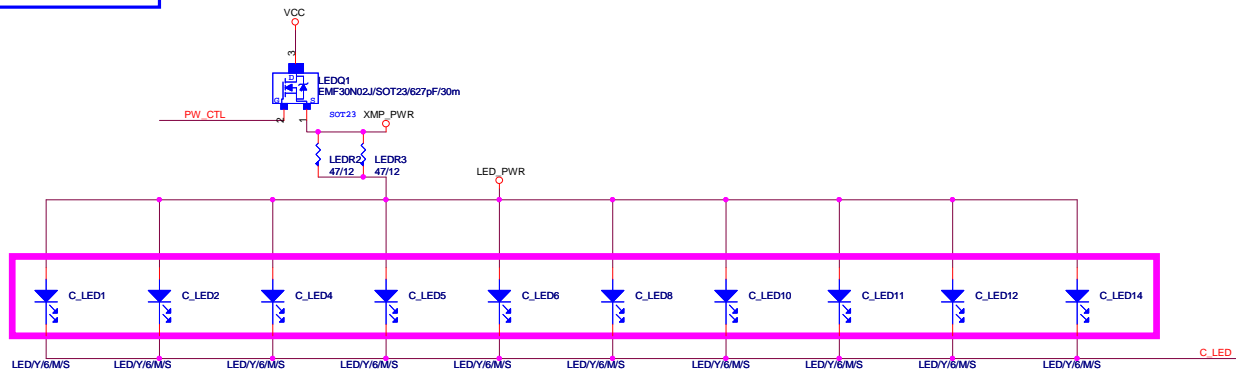


### Frequency change slew rate control



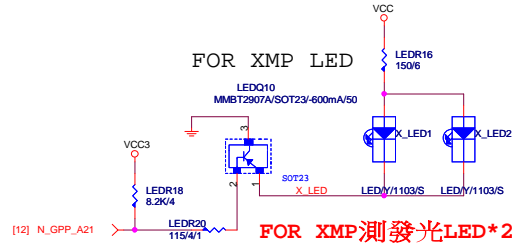
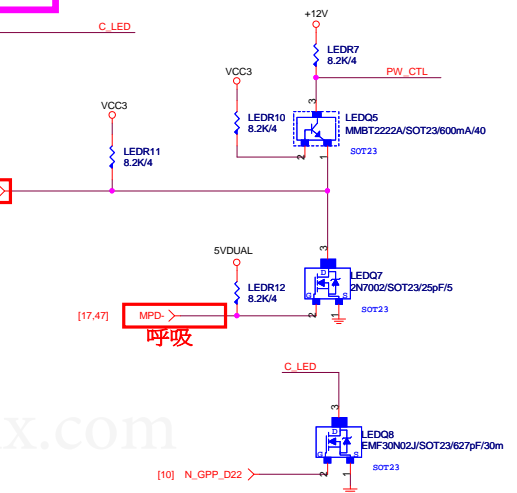
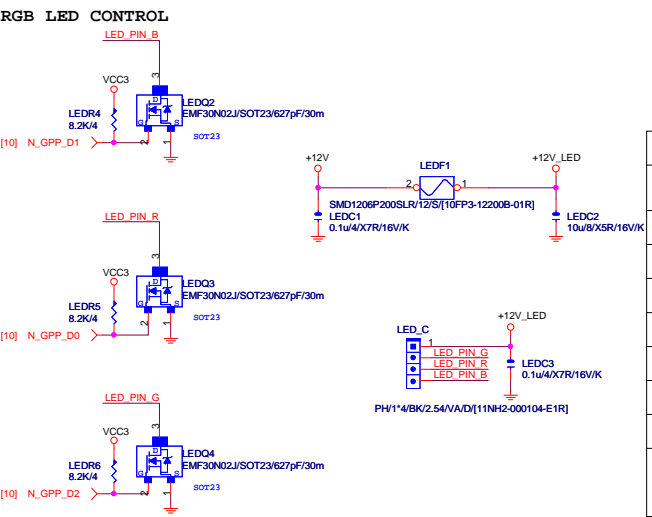
# GIGABYTE

Title			
<b>IDT6V41530_CLK BUFFER</b>			
Size	Document Number	Rev	
Custom	<b>Z370 HD3</b>	<b>1.0</b>	
Date:	Friday, July 28, 2017	Sheet	49 of 53



**Ambient LED Control**

	N_GPP_D22	IO GP91
Still Mode	H	L
OFF Mode	L	L
Pluse Mode	H	BREATH



**三色 LED Control**

	N_GPP_D0 (R)	N_GPP_D2 (G)	N_GPP_D1 (B)
藍	L	L	H
綠	L	H	L
淺綠	L	H	H
紅	H	L	L
粉紅	H	L	H
黃	H	H	L
白光	H	H	H
循環	順序: 藍-綠-淺綠-紅-粉紅-黃-白光 切換間隔時間為 1 秒		



## CLOSE SIO

EMIC1  
100p/4/NPO/50V/J/X

[12,17,30] N\_SLP\_S3 ←

EMIC2  
100p/4/NPO/50V/J/X

[12,17,31,34] N\_S4\_S5 ←

\*Del EMIC3

## CLOSE PCH

EMIC4  
100p/4/NPO/50V/J/X

[4,12] N\_CPUPWROK ←

Vinafix.com

**GIGABYTE™**

Title

**EMI/ESD**Size  
A

Document Number

**Z370 HD3**

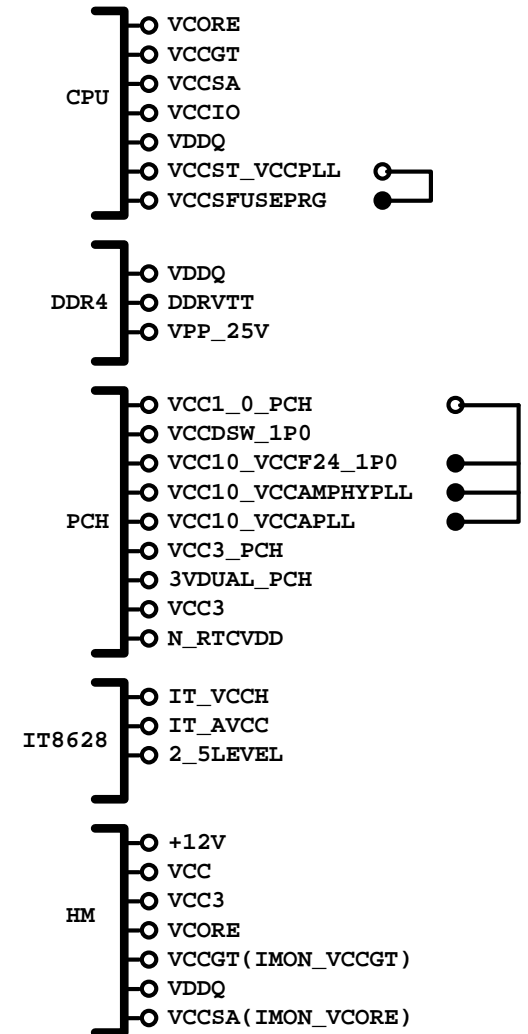
Rev

**1.0**

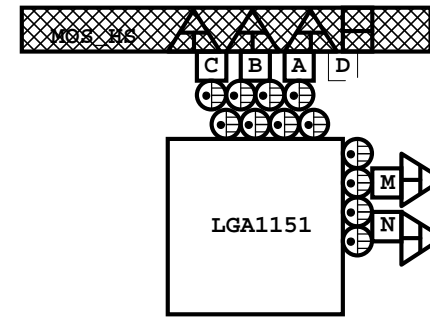
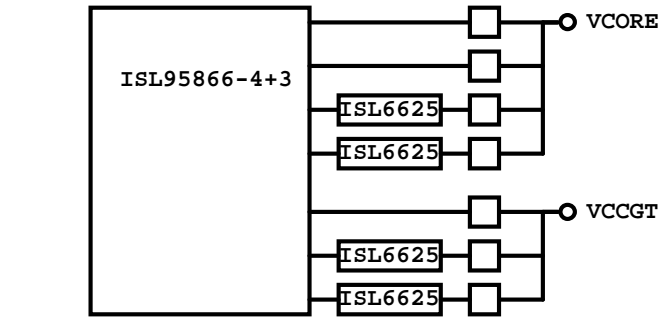
Date: Friday, July 28, 2017

Sheet 51 of 53

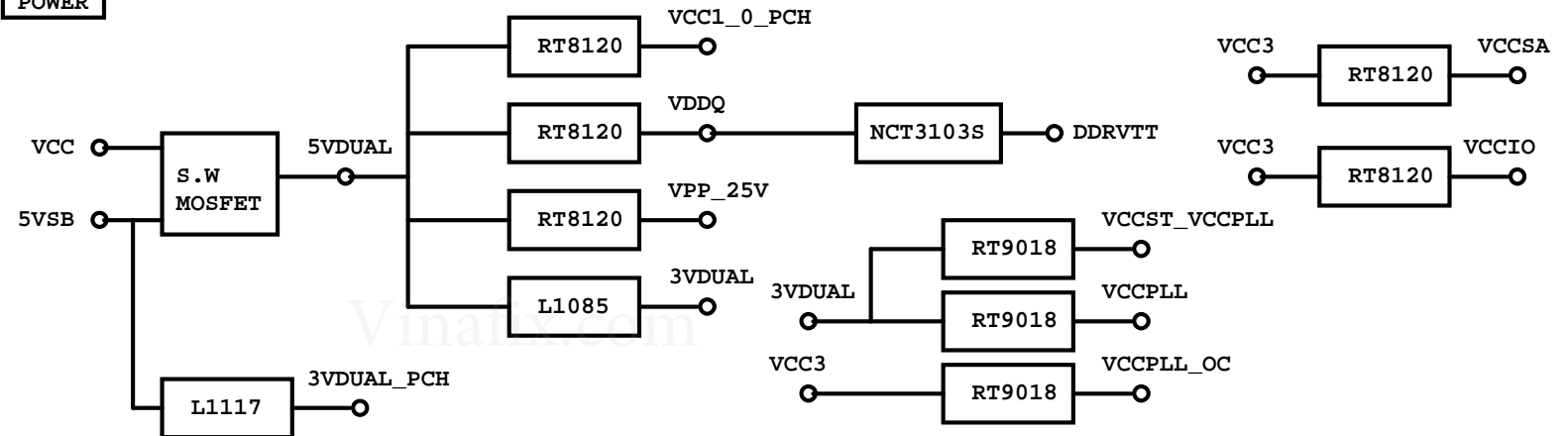
## POWER BLOCK MAP



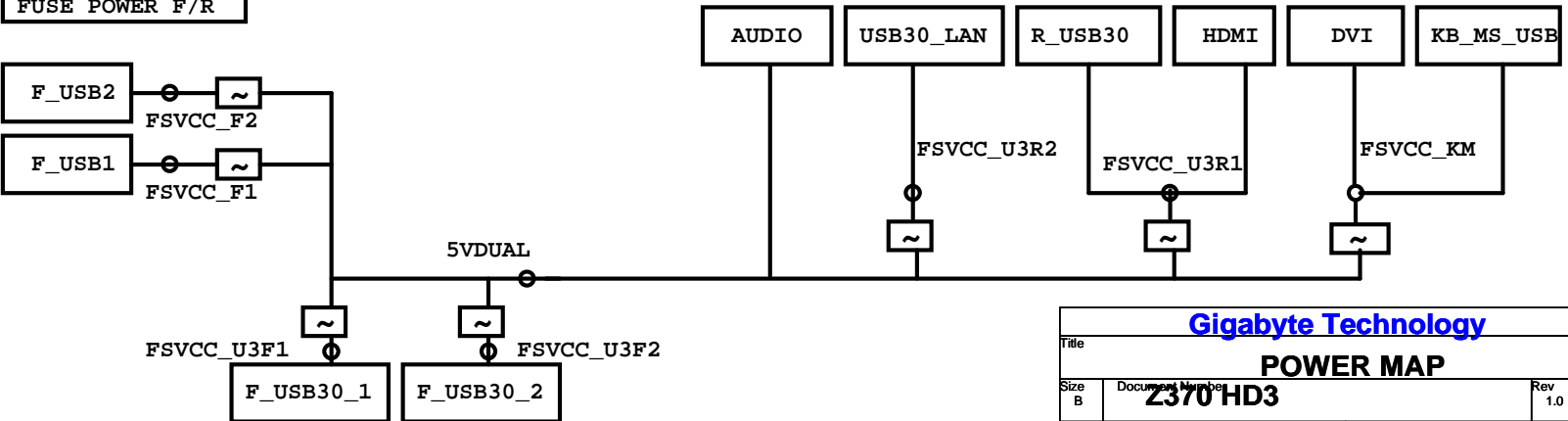
## VCORE/VCCGT



**POWER**



**FUSE POWER F/R**



## Gigabyte Technology

Title			
<b>POWER MAP</b>			
Size B	Document Number <b>Z370 HD3</b>		Rev 1.0
Date:	Thursday, July 27, 2017	Sheet	52 of 53

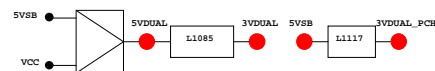
# PCH GPIO LIST TABLE

PIN NAME	PWR	Default	USAGE	NOTE
GPP_A0	MAIN	H-Z	RCIN#	N_KHRST
GPP_A1	MAIN	H-Z	LAD0	N_LAD0
GPP_A2	MAIN	H-Z	LAD1	N_LAD1
GPP_A3	MAIN	H-Z	LAD2	N_LAD2
GPP_A4	MAIN	H-Z	LAD3	N_LAD3
GPP_A5	MAIN	H-Z	LFRAME	N_LFRAME
GPP_A6	MAIN	H-Z	SERIRQ	N_SERIRQ
GPP_A7	MAIN	H-Z	PIRQA#	N_LDRQ0
GPP_A8	MAIN	H-Z	CLKRUN	N_GPP_A8
GPP_A9	MAIN	H-Z	CLKOUT	T_TPMCLK/N_LPC24M
GPP_A11	MAIN	H-Z	PME#	N_P_PME
GPP_A12	MAIN	H-Z	GPI	N_GPP_A12
GPP_A13	MAIN	H-Z	MANR#	N_S_WARN
GPP_A14	MAIN	H-Z	STAT#	N_GPP_A14
GPP_A15	MAIN	H-Z	ACK#	N_S_ACK
GPP_B0	MAIN	H-Z	ZPO	N_DDR_V_SEL
GPP_B2	MAIN	H-Z	GPI	N_VHAIERT
GPP_B3	MAIN	H-Z	GPI	N_GPP_B3
GPP_B4	MAIN	H-Z	GPI	N_GPP_B4
GPP_B5	MAIN	H-Z	GPI	-PCIRX16_PR
GPP_B6	MAIN	H-Z	GPI	-PCIRX1_PK1
GPP_B7	MAIN	H-Z	GPI	-PCIRX1_PK2
GPP_B8	MAIN	H-Z	GPI	-PCIRX4_PK2
GPP_B9	MAIN	H-Z	GPI	-PCIRX1_PK3
GPP_B10	MAIN	H-Z	GPI	LA -CLKREQ
GPP_B12	MAIN	H-Z	SLP_S0	N_SLP_S0
GPP_B13	MAIN	H-Z	PLTRST	N_PPMRST
GPP_B14	MAIN	H-Z	GPO	N_SPKR
GPP_B15	MAIN	H-Z	GPI	N_GPP_B15
GPP_B16	MAIN	H-Z	GPI	N_GPP_B16
GPP_B22	MAIN	H-Z	GPO	N_GPP_B22
GPP_B23	MAIN	H-Z	GPO	N_PCH_RST
GPP_C0	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_C1	MAIN	H-Z	SHBDATA	N_SHBDATA
GPP_C2	MAIN	H-Z	GPO	N_LPCPME
GPP_C3	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_C4	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_C5	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_C6	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_C7	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_C21	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_C23	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_D4	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_D7	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_D8	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_D9	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_D10	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_D13	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_D23	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_E0	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_E1	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_E2	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_E3	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_E4	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_E6	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_E8	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_E9	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_E10	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_E11	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_E12	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F0	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F1	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F2	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F3	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F4	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F5	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F6	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F10	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F11	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F12	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F13	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F14	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F15	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F16	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F17	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F18	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F22	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_F23	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_G11	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_G12	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_G13	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_G14	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_G15	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_G18	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_G19	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_G20	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_G21	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_G22	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_H0	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_H12	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_H19	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_H20	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_H21	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_H22	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_I0	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_I1	MAIN	H-Z	SHBCLK	N_SHBCLK
GPP_I2	MAIN	H-Z	SHBCLK	N_SHBCLK

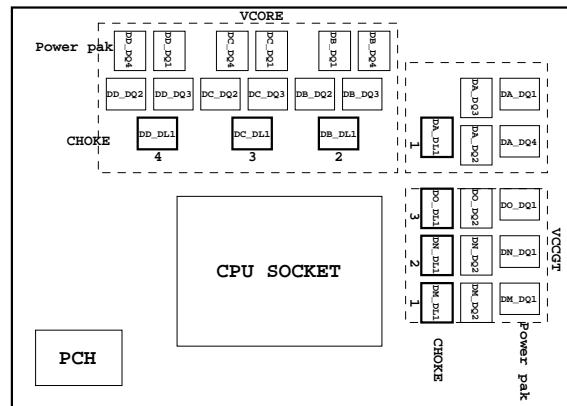
PIN NAME	PWR	Default	USAGE	NOTE
GPP_13	MAIN	H-Z	GPI	N_GPP_13
GPP_14	MAIN	H-Z	GPI	N_GPP_14
GPP_15	MAIN	H-Z	GPI	N_DDBP_CTRLCLK
GPP_16	MAIN	H-Z	GPO	N_DDBP_CTRLCLK
GPP_17	MAIN	H-Z	GPI	N_DDBP_CTRLCLK
GPP_18	MAIN	H-Z	GPO	N_DDBP_CTRLCLK
GPP_19	MAIN	H-Z	GPI	N_DDBP_CTRLCLK
GPP_110	MAIN	H-Z	GPO	N_DDBP_CTRLCLK
GP00	STBY	BATLOW	N_BATLOW	P/U 8.2K 3VDUAL_PCH
GP01	STBY	ACPRESENT	N_GP_D1	P/U 8.2K 3VDUAL_PCH
GP02	STBY	LAM_MAKE	N_LAM_MAKE	P/U 8.2K 3VDUAL_PCH
GP03	STBY	PWRBTN	O_PWRBTN	P/U 8.2K 3VDUAL_PCH
GP04	STBY	SLP_S3	N_SLP_S3	N/A
GP05	STBY	SLP_S4	N_SLP_S4	N/A
GP06	STBY	SLP_S5	N_SLP_S5	N/A
GP08	STBY	SUSCLK	N_SUSCLK	P/D 1.5K GND
GP010	STBY	SLP_S5	N_SLP_S5	N/A
GP011	STBY	LAMPHYC	N_LAN_DIS	N/A

## Super I/O ITE8686 GPIO Table

PIN NAME	USAGE	NOTE
PCIRST3#/GP10/VDIMM_STR_EN	N/A	
PCIRST2#/GP11	O_PCH_RST	
PCIRST1#/GP12	O_PPMRST2	
SVC/PECI_RQT/GP14	N_THERMTRIP	
SLP_SUS#/PCIRSTIN#/CIRT2/GP15	N_GPP_B20	
PS1_L/FAN_CLT5/CIRKX2/GP16	<a href="#">PIN</a>	
R12#/GP17	IO_GP17	
THR_PWM_CTS2#/GP20	<a href="#">PIN</a>	
IO_SMI#DCD2#/GP21	<a href="#">PIN</a>	
SPI_S1/GP22	-ICH_SPI_CS	
DPWRCK/CPU_PG/GP23	N_PCH_DPWRCK	
FAN_TAC5/RTS2#/GP24	<a href="#">PIN</a>	
FAN_TAC4/D8R2#/GP25	FANIO4	
INV_OUT1/OUT2/GP26	MB_ID2	
INV_IN1/SIN2/GP27	BEEP-	
ATXPG/GP30	PWOK_IO	
CT81/GP31	CT81-	
OCMDT3/R11#/GP32	R11-	
OCMDT2/DCD1#/GP33	DCD1-	
VTT_PMRGD/GP34	VTT_PMRGD	
VCC18_EN/GP35	VCC18_EN	
FAN_CTL3/GP36	FANPWM3	
FAN_TAC3/GP37	FANIO3	
3VSBSEN/GP40	<a href="#">PIN</a>	
OCMDT1/SIN1/GP41	RXD1	
GP42/SCK/FAN_CTL4	FANPWM4	
FANSEN/GP43	-PWRBTW	
PWRCKN/GP44	O_PWRBTW	
OCMDT0/D8R1#/GP45	D8R1-	
CE2_N/GP47/JP6	CEB_N	
GP50/JP1	O_TPMCLK	
FAN_CTL2/GP51	FANPWM2	
FAN_TAC2/GP52	FANIO2	
SUSCK/GP53	N_S4_S5	
PME#/GP54	N_LPCPME	
RSMRST#/CIRKX1/GP55	O_RSMRST	
MCLK/FAN_TAC6/GP56	MCLK	
MDAT/FAN_CTL6/GP57	MDAT	
KCLK/GP60	KCLK	
KDAT/GP61	KDAT	
KRST#/GP62	N_KRST	
HOLD_B#/GP63	-SPI_HOLD_B	
HOLD_B#/GP64	-SPI_HOLD_M	
VLDI_EN/PCH_D0/GP65	<a href="#">PIN</a>	
VCC1_05_EN/GP66	VCC1_0_EN	
GP67	N_RTCRST	
USB_F81/PD0/GP70	PD0	
USB_F82/PD1/GP71	PD1	
USB_F83/PD2/GP72	PD2	
USB_F83/PD3/GP73	PD3	
USB_F85/PD4/GP74	PD4	
USB_F86/PD5/GP75	PD5	
USB_F87/PD7/GP76	PD6	
USB_F88/PD8/GP77	PD7	
LS_IN1/SLCT/GP80	SLCT	
LS_OUT1/PE/GP81	PE	
LS_IN2/BSY/GP82	BUSY	
LS_OUT2/ACK#/GP83	ACK-	
IPHONE_CHARGE#/SLIN#/GP84	SLIN-	
OC_IN/INIT#/GP85	INIT-	
OC_OUT/AFD#/GP86	AFD-	
USB_OC2/STB#/GP87	STB-	
DDR_EN/GP90	MA_EN	
PWRLED/GP91	MPD-	
HOLD_OUT/GP92	<a href="#">PIN</a>	
HOLD_IN/GP93	IO_GP93	
PROCHOT#/GP94	-PROCHOT_CON	
CPUPWRGD/GP95	<a href="#">PIN</a>	
PCH_VRMPPWRGD/GP96	N_PCH_VRMPPWRGD	
VR_RDY/GP97	VR_RDY	



PWM各相位的擺法如下:



BIOS超電壓對應表:

線路圖名稱	BIOS選項
Vcore	CPU Vcore
VCCGT	CPU Graphic Voltage
VCCIO	CPU VCCIO
VCCSA	CPU System Agent Voltage
VCCST_VCCPLL	VCC Substained
VCCPLL	VCCPLL
VCCPLL_OC	VCCPLL_OC
VCC1_0_PCH	PCH core
VDDQ	DRAM voltage
VPP_25V	DRAM VPP voltage
DDRVT	DRAM Termination

散熱模組料號:

Z370-HD3 :  
 TMOS  
 12SP2-S09426-21R/22R/23R  
 RMOS  
 12SP2-S08026-21R/22R/23R  
 PCH\_HS  
 12SP2-S08607-01R/02R/03R  
 12SP2-PT\*表示組合料號(2合1或3合1料件)

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU_FAN	FANPWM1	VCC	FANIO1	IT8686
	FAN_C_VOUT	N/A	N/A	NCT3947
SYS_FAN1	FANPWM2	VCC	FANIO2	IT8686
	FAN1_VOUT	N/A	N/A	NCT3947
SYS_FAN2	FANPWM3	VCC	FANIO3	IT8686
	FAN2_VOUT	N/A	N/A	NCT3947
SYS_FAN3	FANPWM4	VCC	FANIO4	IT8686
	FAN3_VOUT	N/A	N/A	NCT3947